Physics Challenges Facing the Semiconductor Industry

Based on the

International Technology Roadmap for Semiconductors

Alain C. Diebold

INTERNATIONAL SEMATECH

Acknowledgements

- **PY Hung, Hugo Celio, Jimmy Price**
- **Mark Bohr Intel**
- **Novjot Chhabra and Ken Monnig**
- **ITRS Metrology US and International TWGs**

- **References**

  - International Technology Roadmap for Semiconductors
  - HJ Levinson, Principles of Lithography
  - C Steinbruchel and BL Chin - Copper Interconnect Technology
  - SM Sze – High Speed Semiconductor Devices
  - How CMOS works
    http://tech-www.informatik.uni-hamburg.de/applets/cmos/cmosdemo.html
  - Fabrication Process
    http://jas.eng.buffalo.edu/education/fab/invFab/

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AGENDA

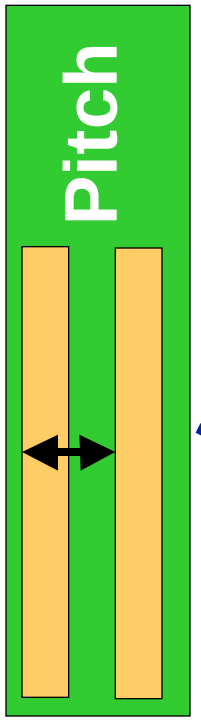
- The ITRS Challenge
- Litho Processes and Metrology
- FEP Processes and Metrology
- Interconnect Processes and Metrology
- Materials Characterization

Terminology

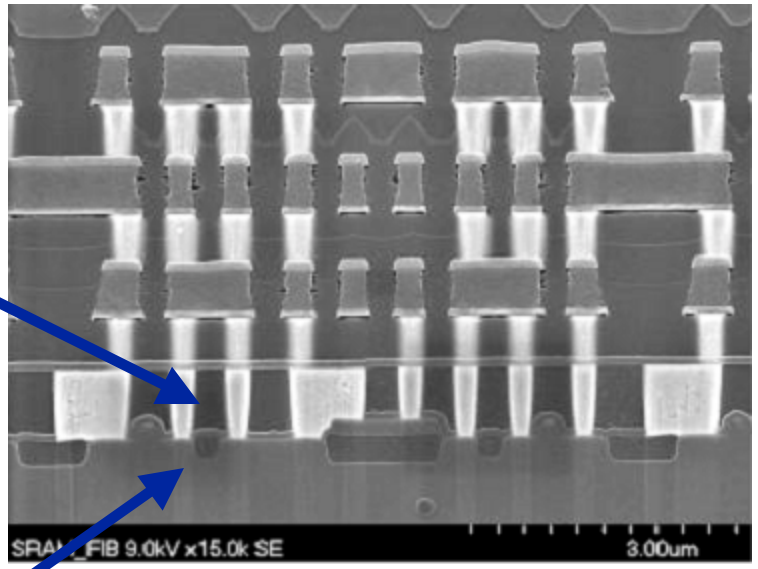
0.065 µm High-performance Micro- Processor

pitch =
distance between closest spaced metal interconnect lines at first level of DRAM

Top View



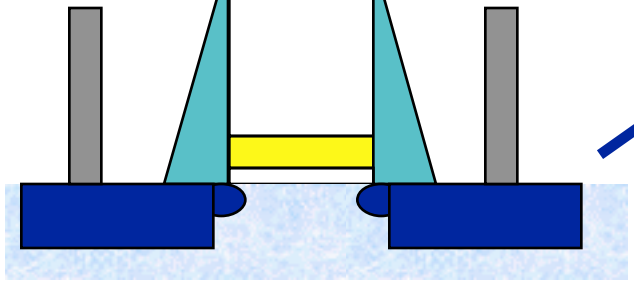
Side View



CD

Gate

source **drain**



Transistor

Figure courtesy Bryan Tracy

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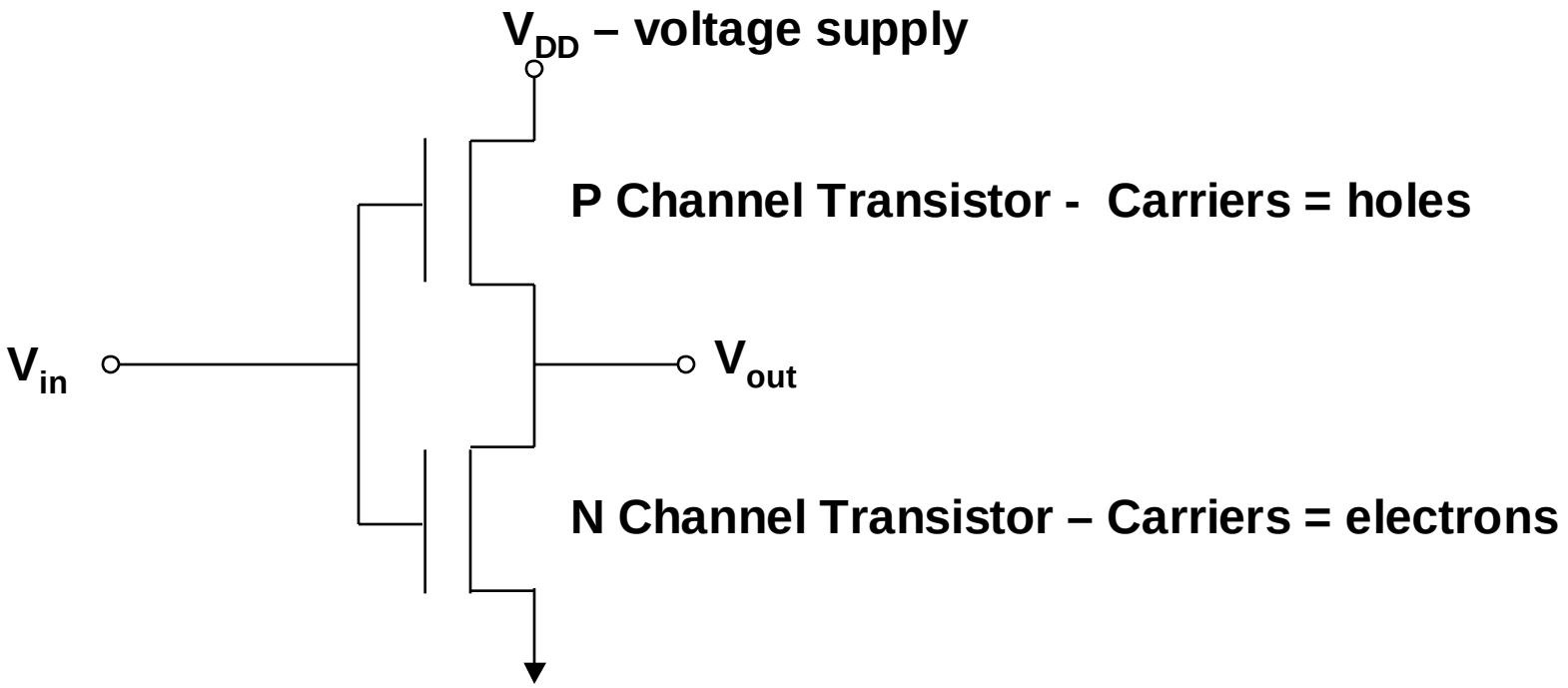
CMOS Inverter

Complementary
Metal Oxide Semiconductor Field Effect Transistor



Digital -- 0 and 1

At V_{in} = 0, V_{out}/V_{DD} = 1

As input voltage V_{in} goes from 0 to 1 = V_{in}/V_{DD} ⇨ V_{out}/V_{DD} = 1

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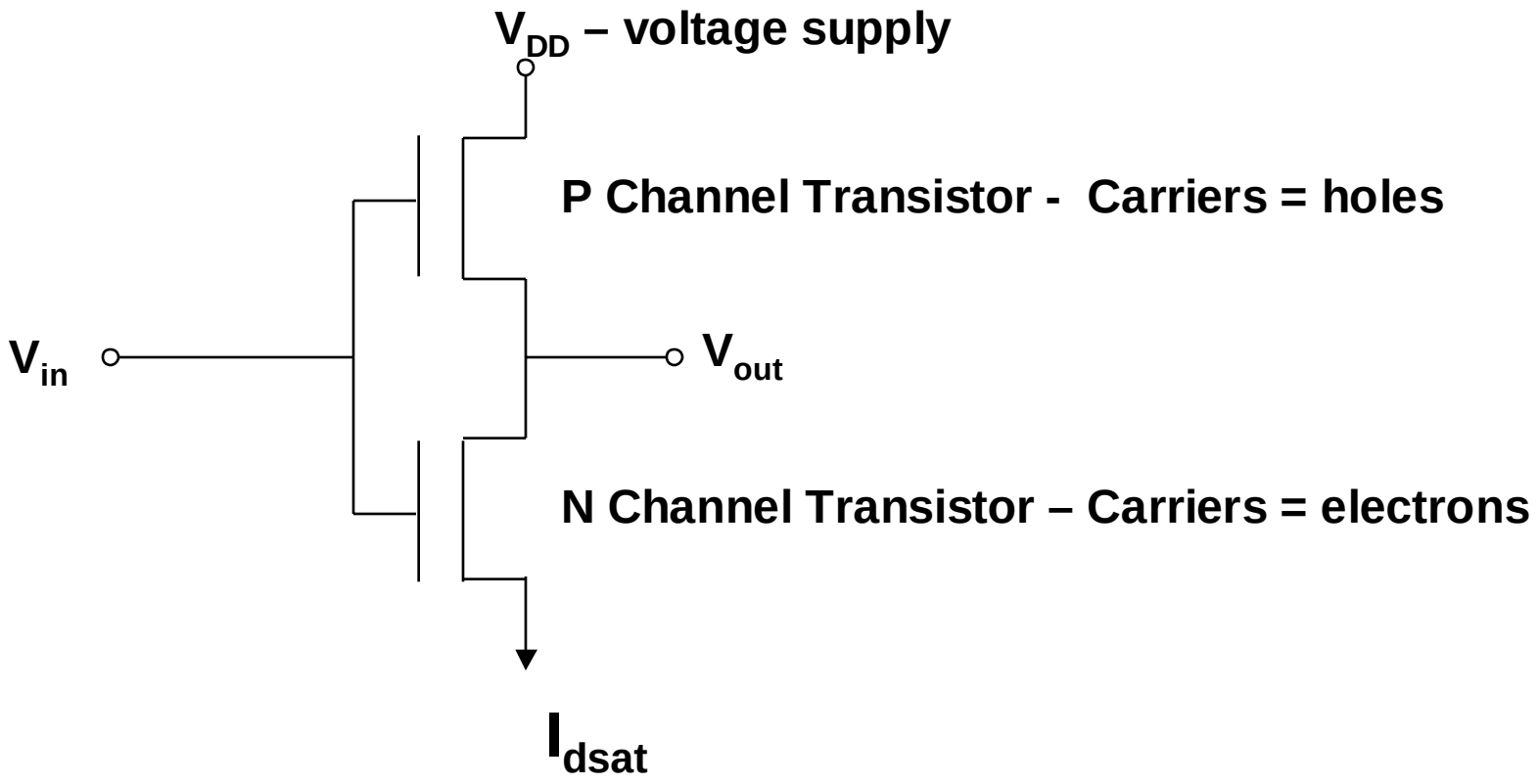
CMOS

Switching Speed $\tau \sim 1/I_{dsat}$
governed by Saturation Drive Current



$I_{dsat} = (W/2L_g)\ (3.9K_oA)\ (T_{EOT,INV})^{-1}\ \mu_{eff}\ (V_G-V_T)^2$ (long-channel, ideal)

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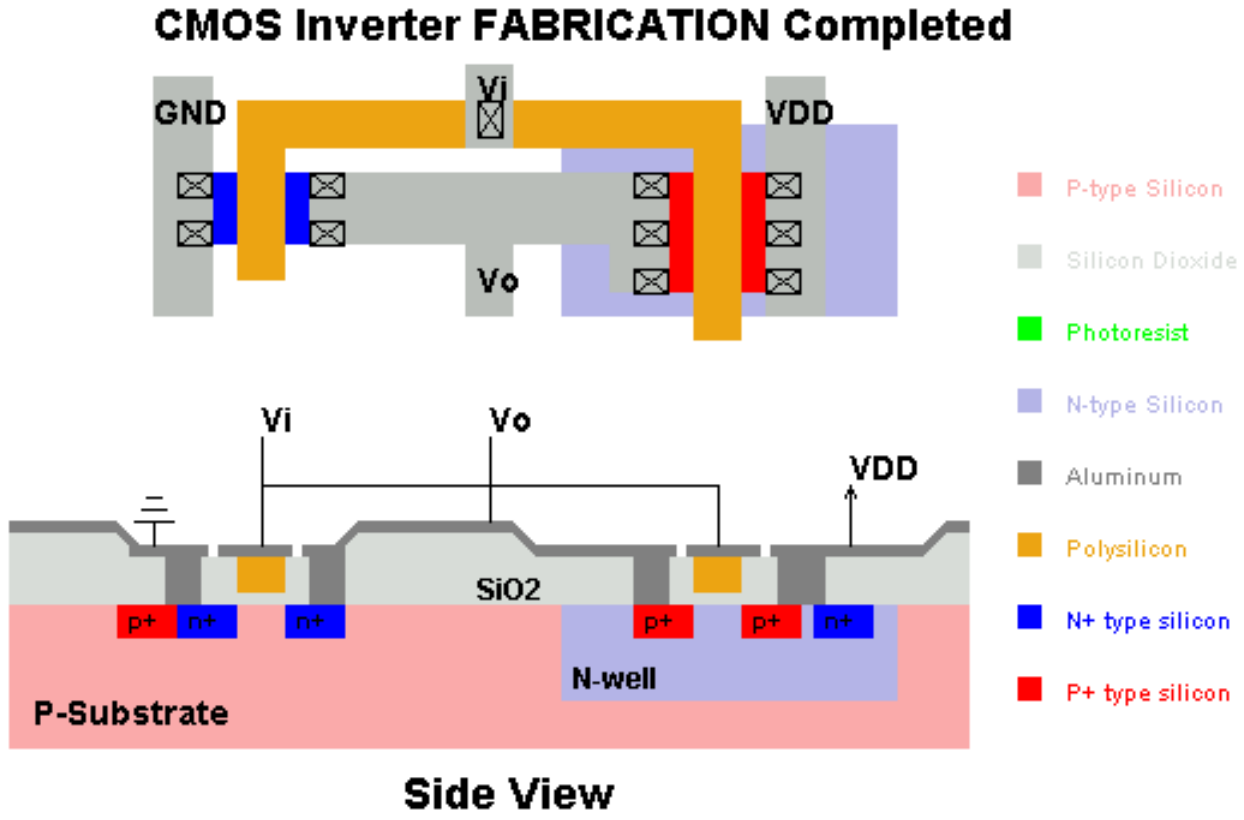
CMOS
What it looks like



http://jas.eng.buffalo.edu/education/fab/invFab/

See the process in action

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Terminology

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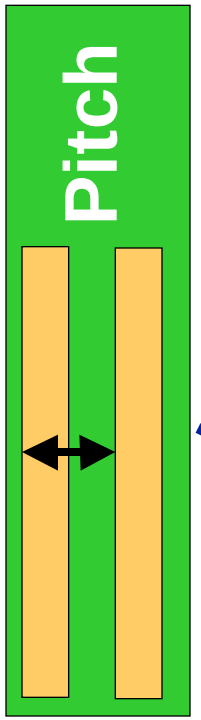
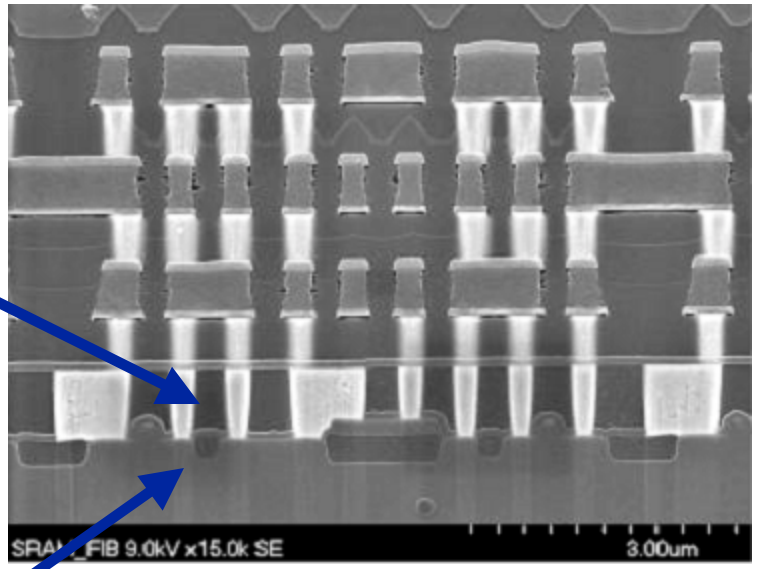
Top View



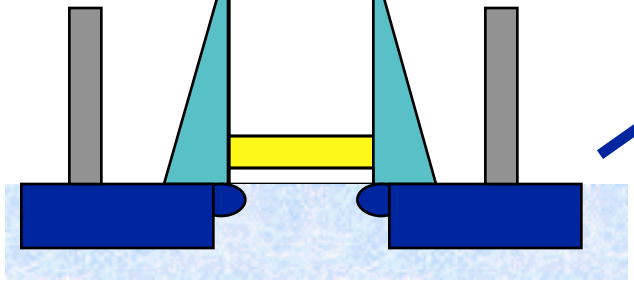
Side View



CD

Gate

source **drain**



Transistor

Figure courtesy Bryan Tracy

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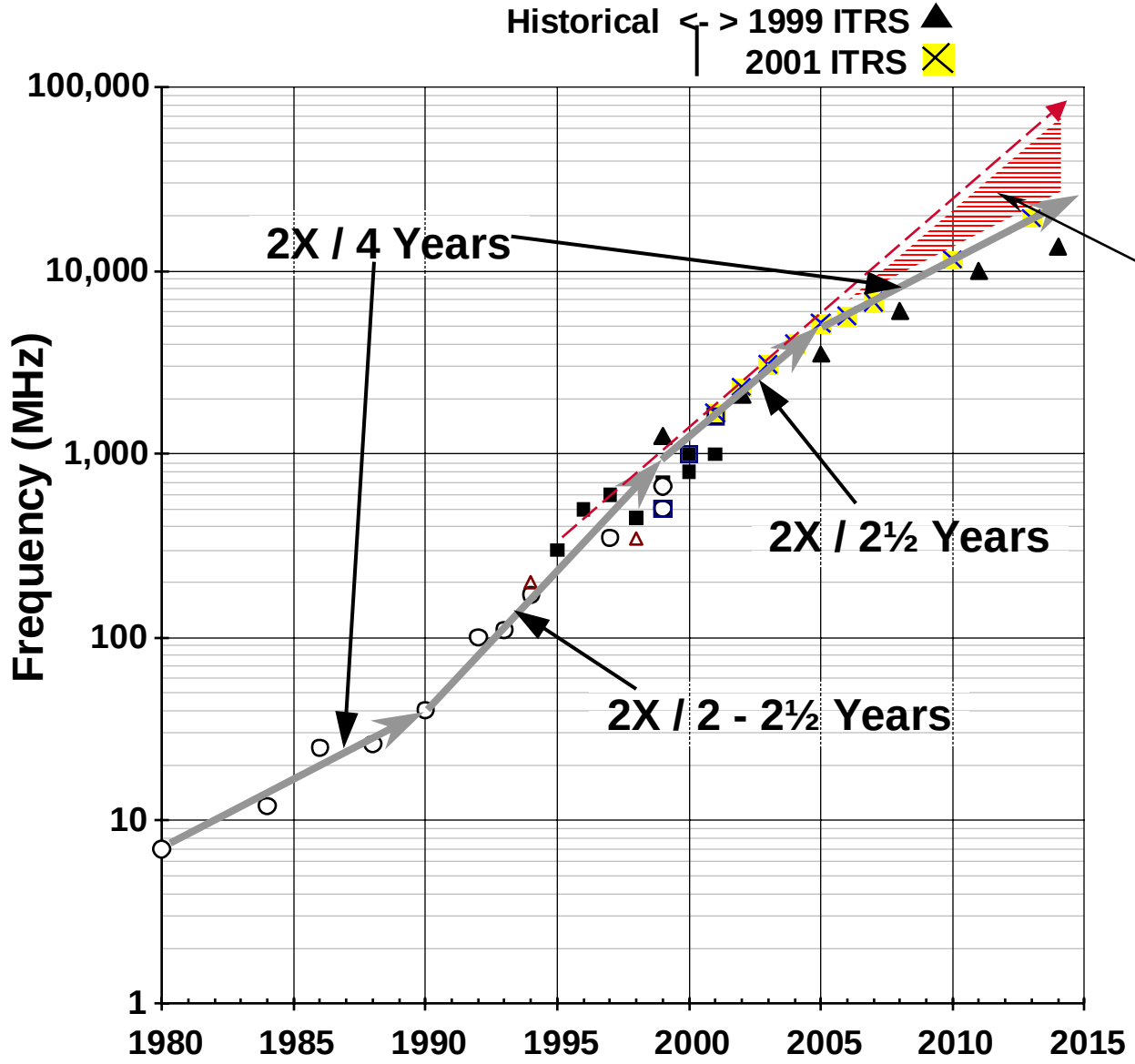
MPU Clock Frequency Actual vs ITRS



Sources: Sematech, 2001 ITRS ORTC

Goal: Increase Speed by 2x Speed/2-2.5 years

Actual Scaling Acceleration, Or Equivalent Scaling Innovation Needed to maintain historical trend

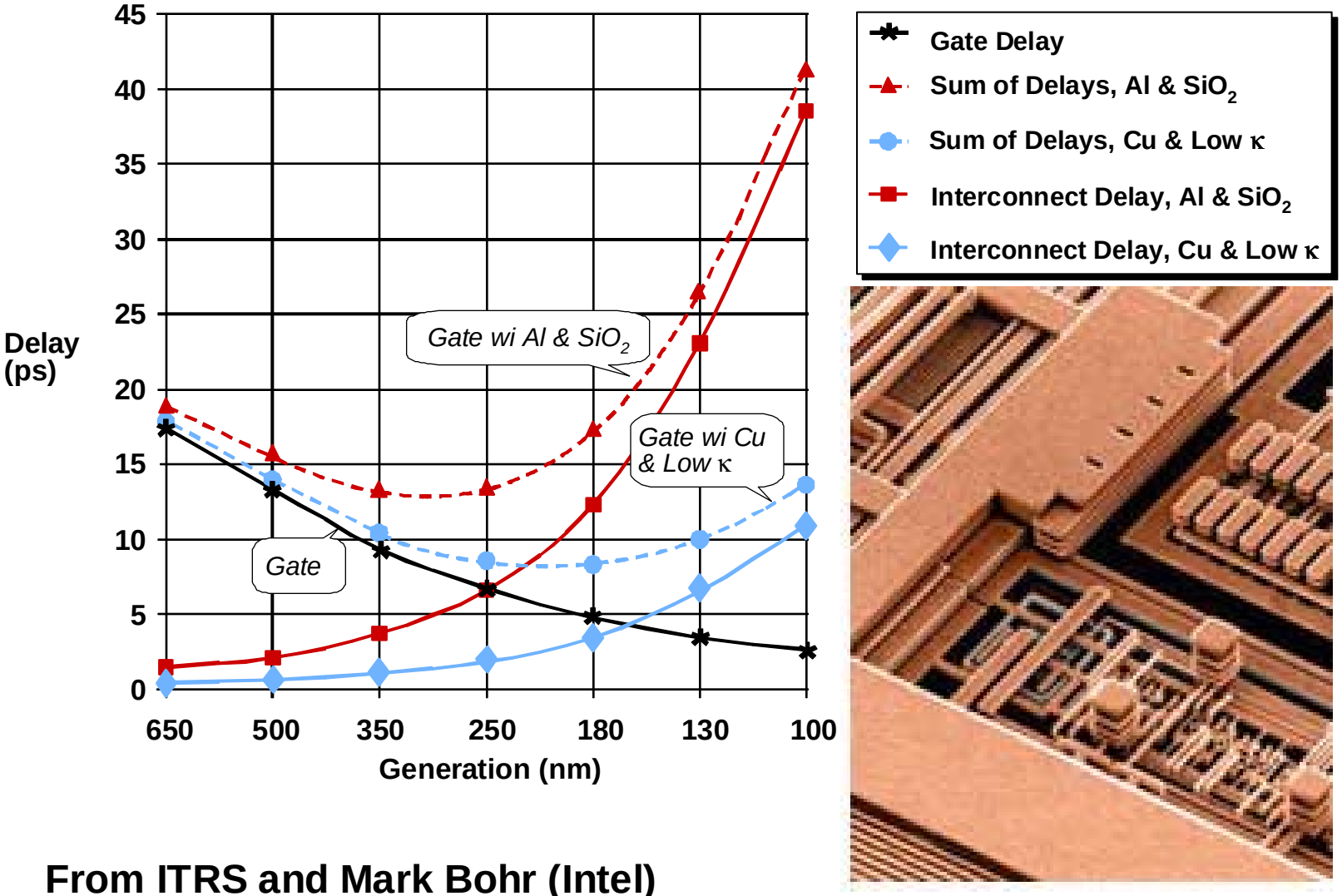
MPU Clock Frequency Historical Trend:

Gate Scaling, Transistor Design contributed ~ 17-19%/year

Architectural Design innovation contributed additional ~ 21-13%/year

Transistor and Interconnect Delays

SPEED / PERFORMANCE ISSUE *The Technical Problem*



From ITRS and Mark Bohr (Intel)
Figure from IBM

INTERNATIONAL SEMATECH

Speed of Transistor

Transistor Gate Delay, τ, decreases as CD decreases but Gate Dielectric must also decrease in thickness.

$\tau = C_{load} V_{dd} / I_{dsat}$ $C_{load} = C_{ox} + C$

V_{dd} power supply voltage

I_{dsat} saturation Drive current

I_{dsat} ↑ as L_g gate length ↓

Sounds Easy

- Just decrease the Gate length &/or increase mobility

TROUBLE As dielectric thickness decreases leakage current increases

$I_{dsat} = (W/2L_g)\ (3.9K_oA)\ (T_{EOT,INV})^{-1}\ \mu_{eff}\ (V_G-V_T)^2$ (long-channel, ideal)

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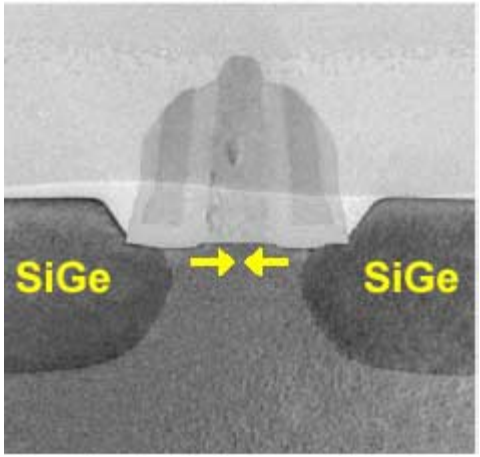
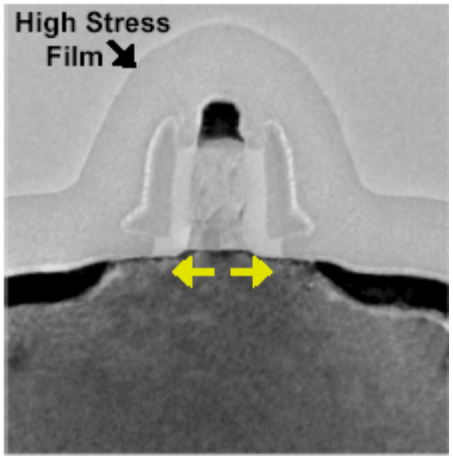
High Volume IC s use CMOS w/ Locally Strained Si

Strained Si substrates not used



PMOS
Compressive Strain
increased hole mobility



45 nm NMOS
Tensile Stress SiN Layer
increased electron mobility

From T. Ghani, et. al., IEDM 2003, p 978.
Courtesy Intel Not for reproduction

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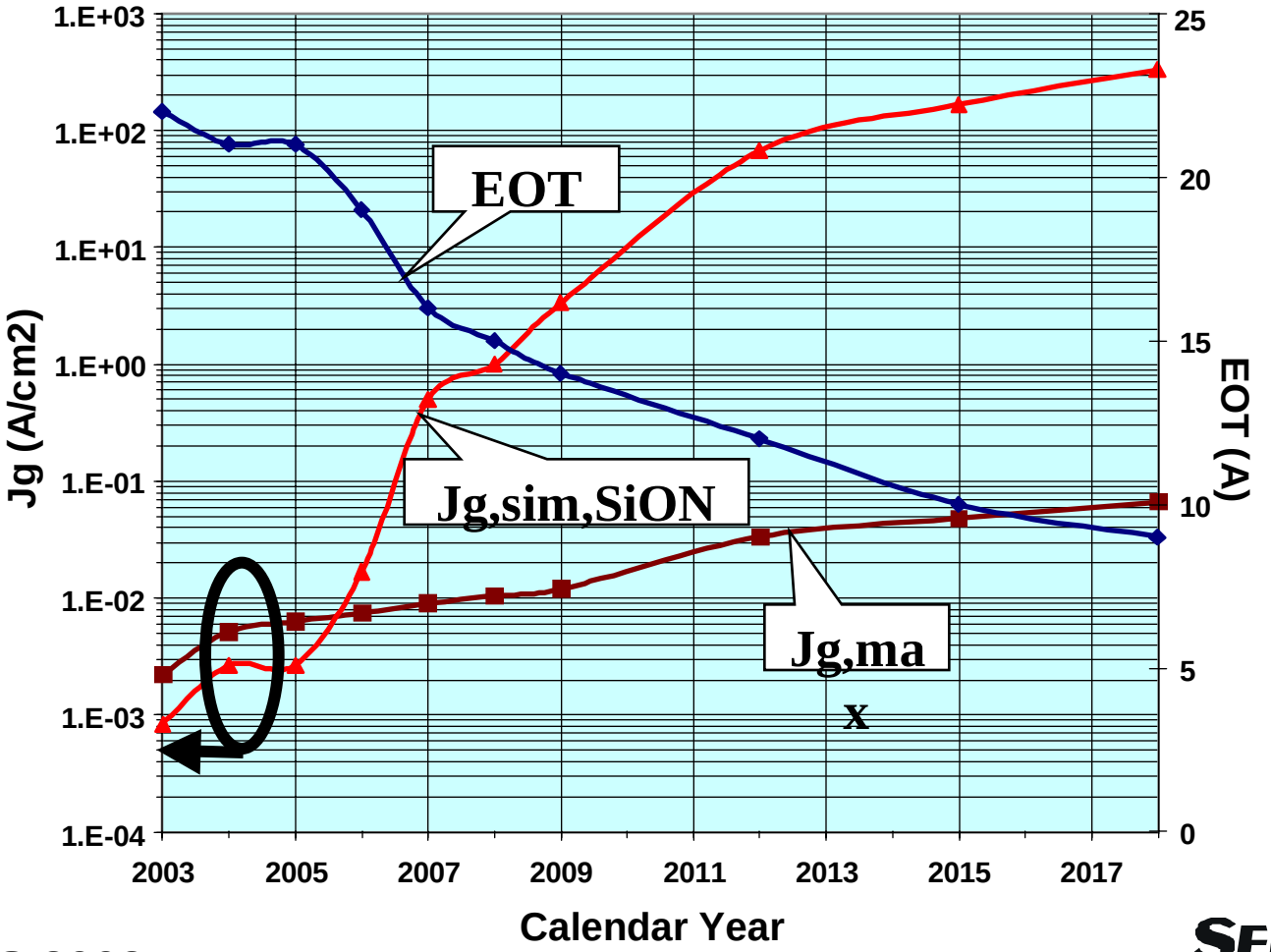
Problem Leakage Current Increases as SiO_2 Gate Dielectric thickness decreases



PIDS ITRS 2003

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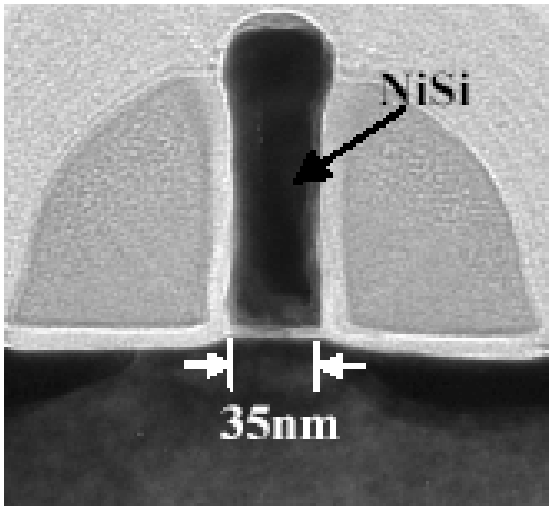
Near Term Solution New Materials

Dielectric Material **w/ High k**
Poly Si Gate **w/ Metal Gate**
Transistor Channel **w/ Strained Si**



Q. Ziang, et al., AMD
VLSI 2003
NMOS w/Strained Si

GL = 25 to 35 nm

EOT = 1.3 nm
SOI Si channel = 8.5 – 10 nm.

PMOS I*dsat* = 789 μA/μm
@ Vgs - Vt = 1.25 V + V_{dd} = 1.5 V
.
NMOS I*dsat* = 1006 μA/μm
@ Vgs - Vt = 1.3 V + V_{dd} = 1.5 V.

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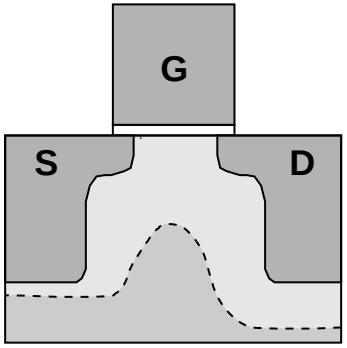
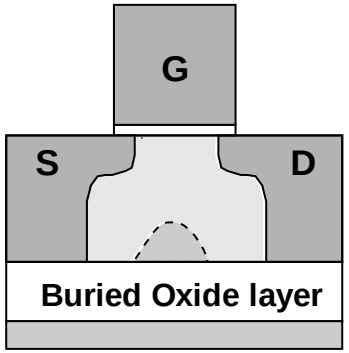
Long Term Solution
New Type of Transistor & Wafer

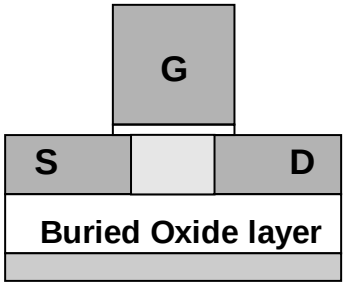
Bulk MOSFET



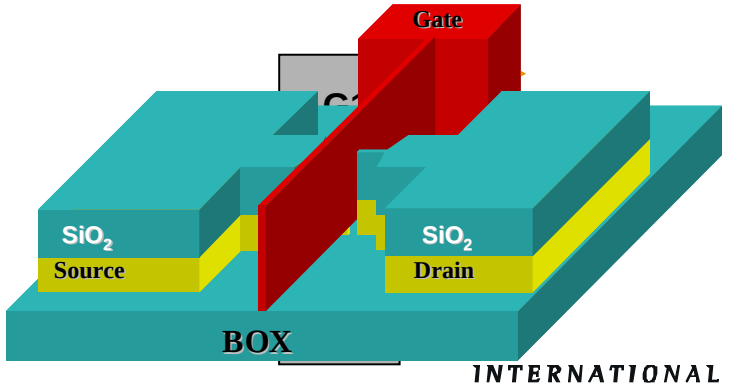
Partially-Depleted SOI



Ultra-Thin Body SOI



Double-Gate MOSFET



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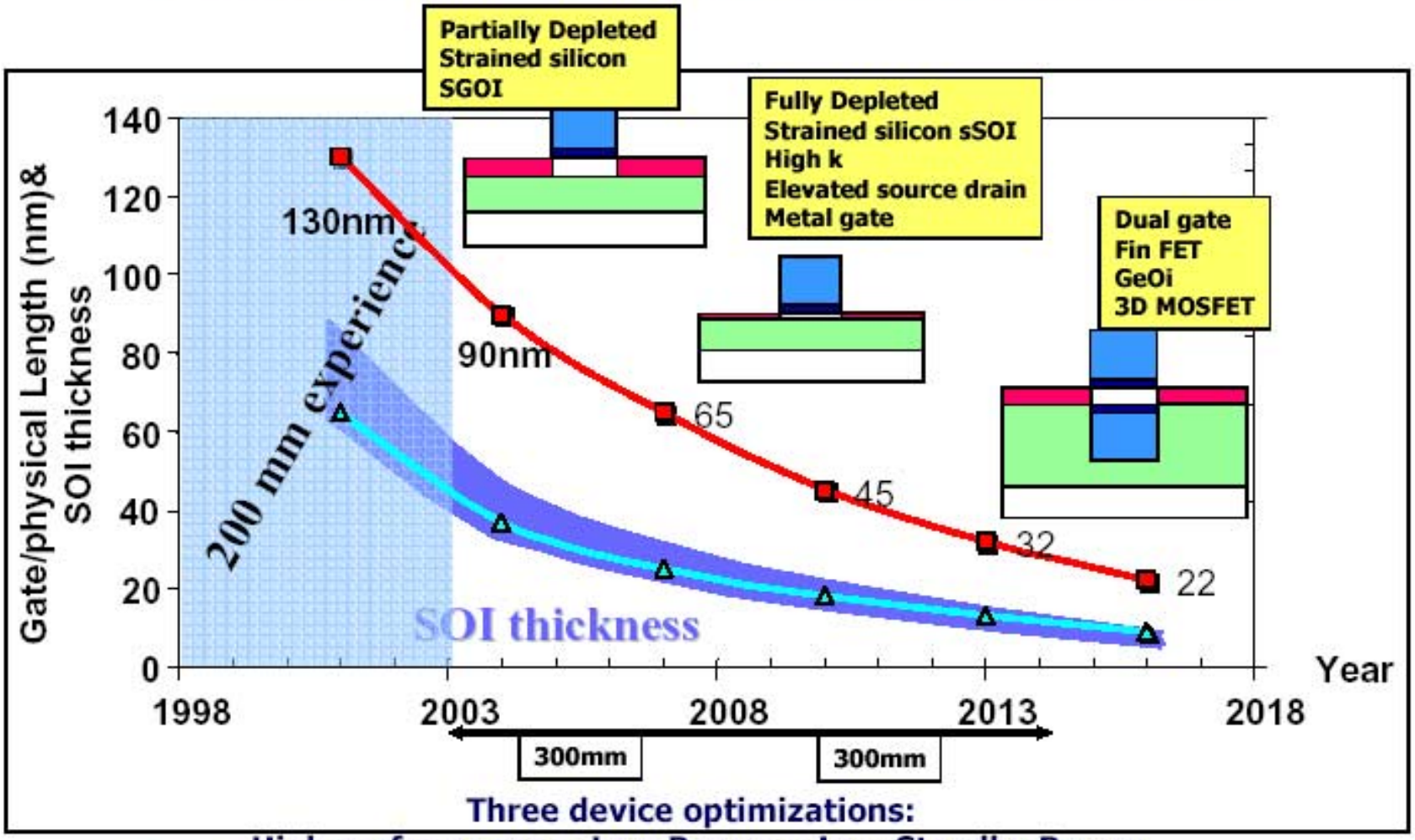
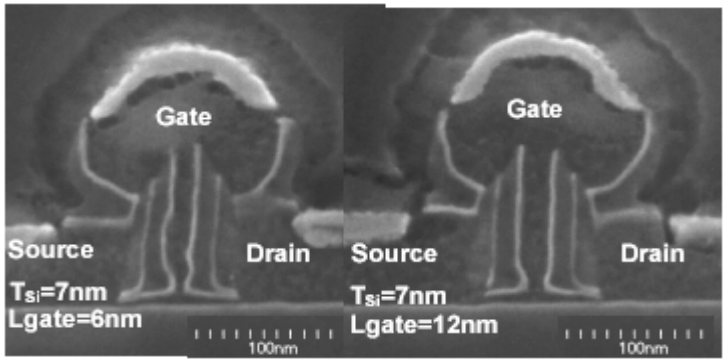
SOI Evolution courtesy SOITEC



ITRS International Technology Roadmap for Semiconductors

IC R&D in Nano Transistors



GL = 6 nm

EOT = 1.2 nm

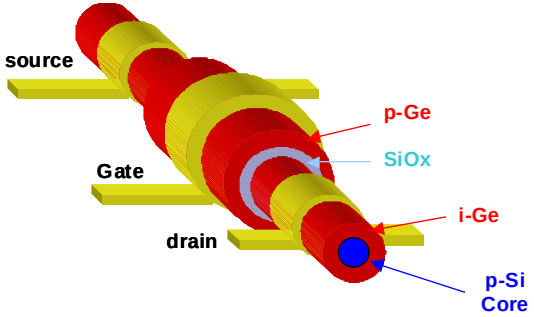
SOI Si channel = 4.6 nm

PMOS *Idsat* = 130 μA/μm

@ Vgs - Vt = 1.65

V + V_{dd} = 1.5 V

VS



p-Si core/i-Ge/SiO_x/p-Ge

GL = 1500 nm

EOT ~ 0.4nm

I*dsat* = 1 μA/μm

@ V_{dd} = 1 V

Bruce Doris IBM
IEDM 2002 and 2003

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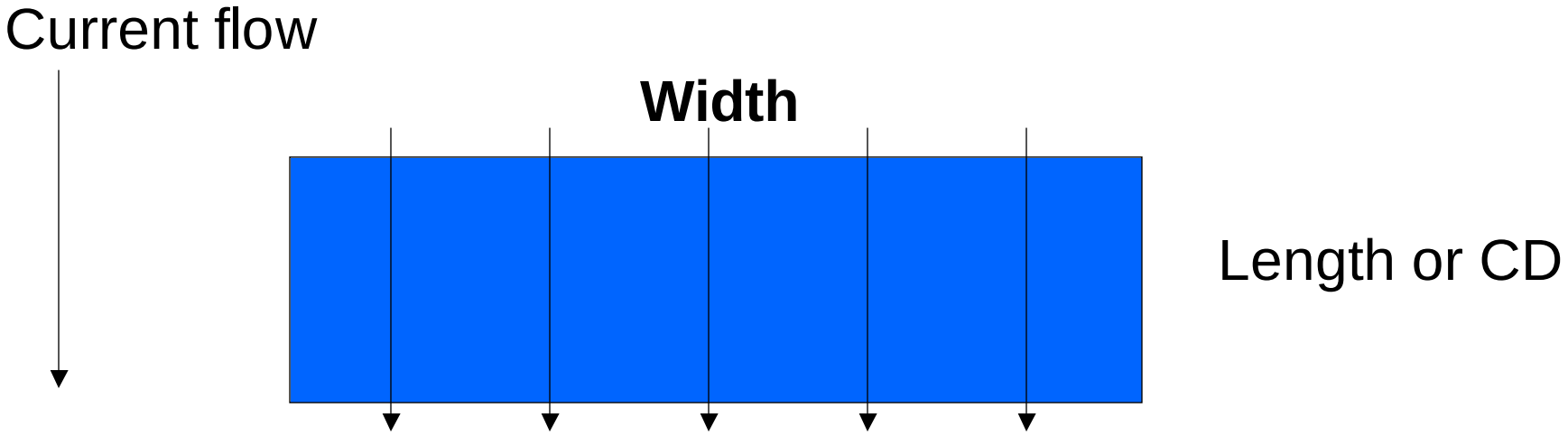
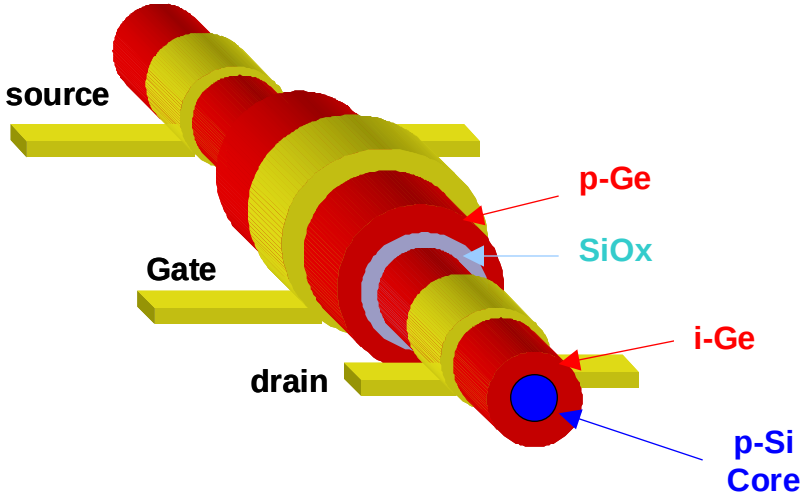
How do we compare Nano-Tech Transistors with Conventional Transistors?



ITRS requires high performance transistors for the next 15 years have a current of from ~ 1 to ~ 2 x 10^{-3} amp/μm

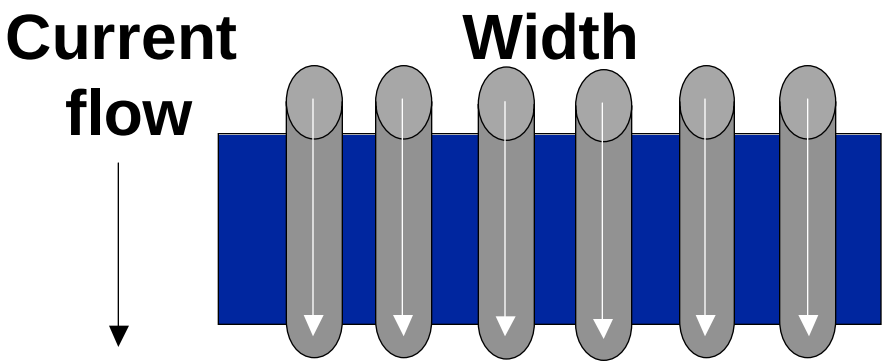
NMOS ~ 1mA / μm
PMOS ~ 0.5 to 0.7 mA / μm

Saturation Current is normalized by gate width W



p-Si core/i-Ge/SiO_x/p-Ge
GL = 1500 nm
EOT ~ 0.4nm
Observed range of 1 to 5 µ A @ 1V

Diameter without metal connection to Ge gate is 50 nm



1 milli-amp of current/ µm needed to meet performance requirements

1 x 10^{-3} amps = 200 nanowire transistors x 5000 nano Amps/transistor

This would require 200 nanowires in 1 micron width = 50 nm / nanowire with I*dsat* = ~ 5 **µA/µm of each nanowire transistor @ $1V_{dd}$**
Or
1000 nano Amps/transistor x 1000 nanowire transistors with 10 nm space
With I*dsat* = ~ 1 **µA/µm -------- an impossible pitch**

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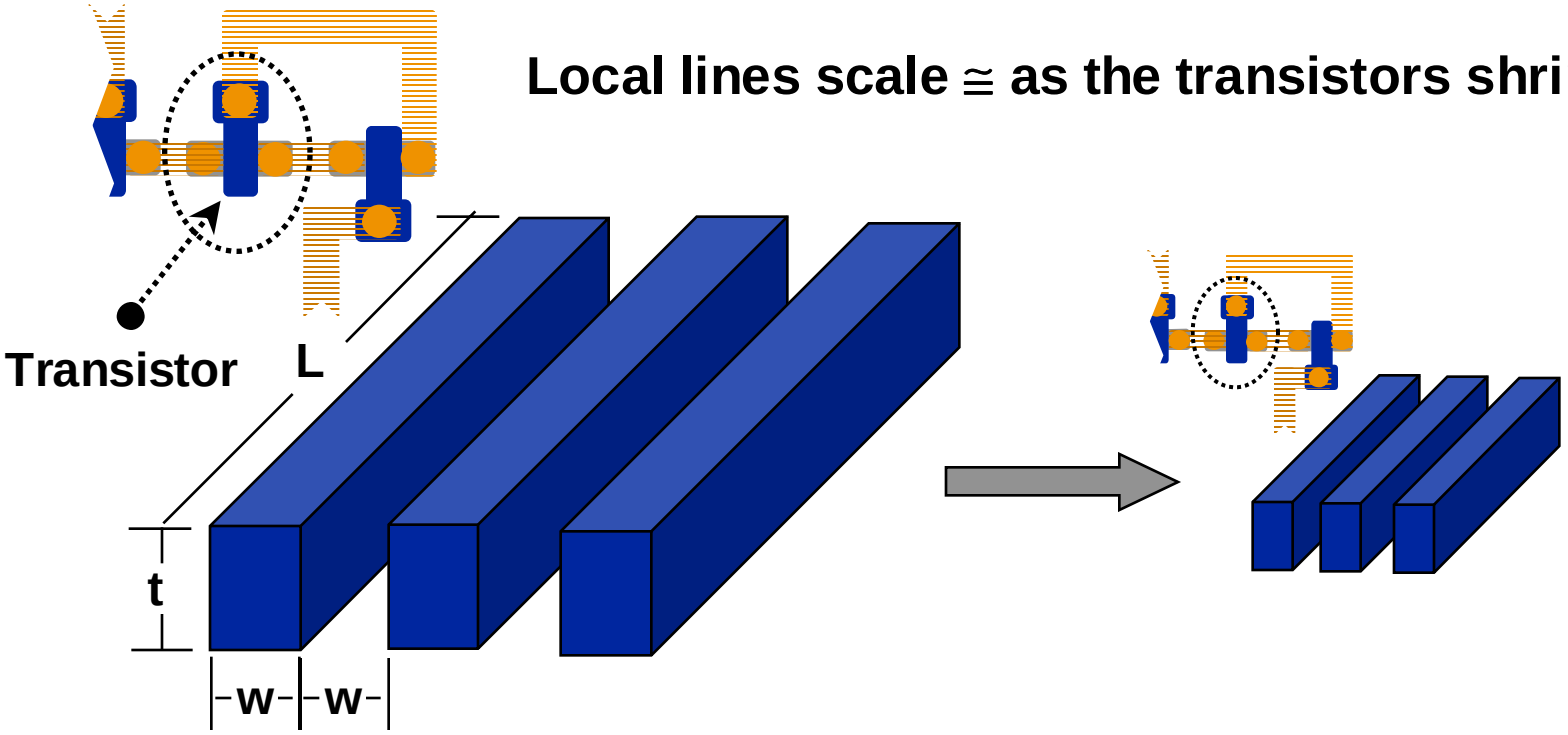
Interconnect Delay :LOCAL LINE SCALING



Local lines scale ≅ as the transistors shrink.

Local conductor lines get smaller in cross-section, spacing <u>& length</u>.

$$\text{RC Delay} \cong \rho\, \varepsilon \frac{L^2}{w^2}$$

Both L&W Scale ≅ the Same

Thanks to Novjot Chhabra

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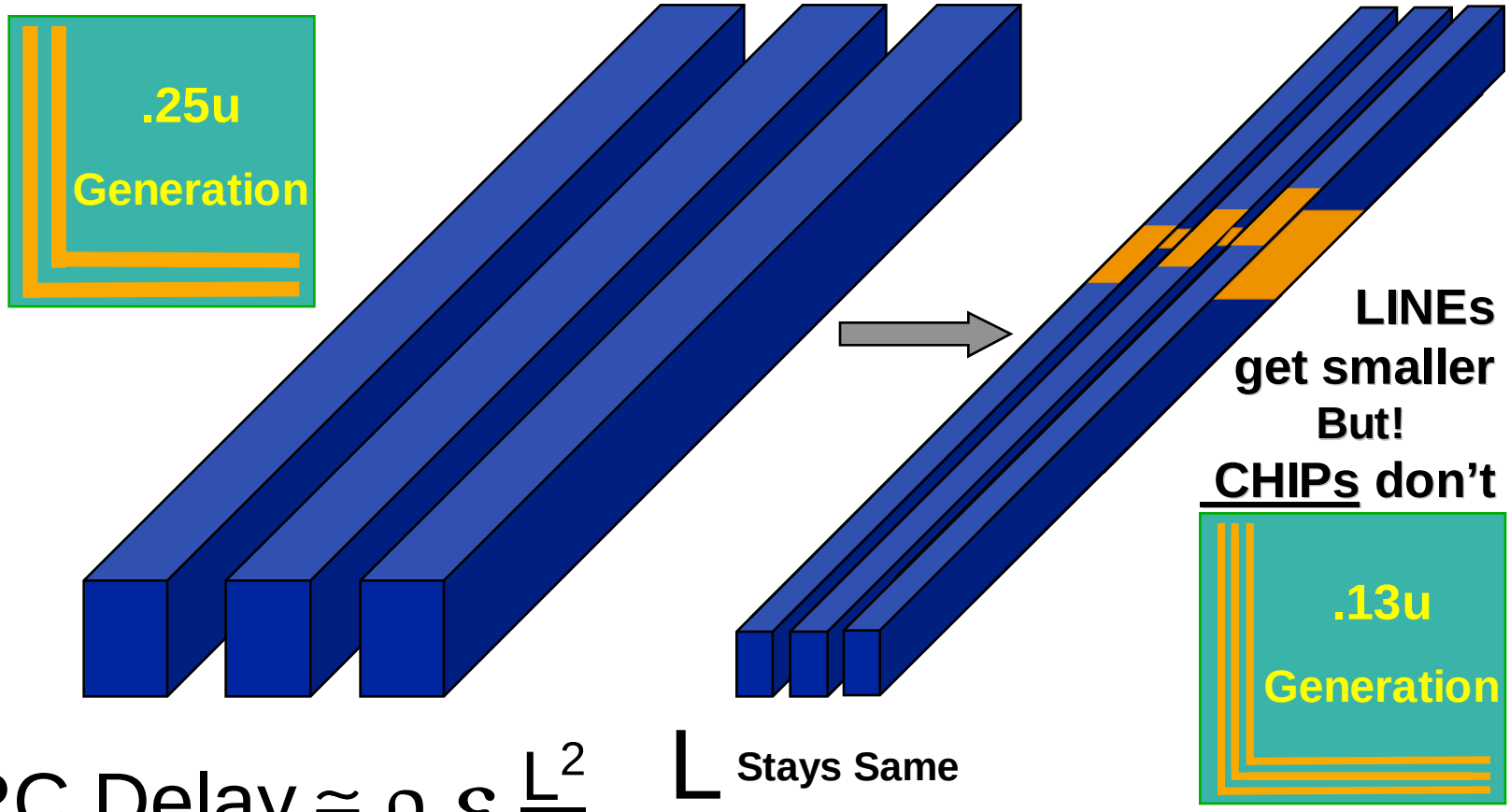
Interconnect Delay :GLOBAL LINE SCALING

Global conductor lines getting smaller in cross-section but *NOT* in length. Signal delay is growing exponentially!



$$\text{RC Delay} \cong \rho\ \varepsilon\ \frac{L^2}{w^2}$$

L Stays Same

W ⬇ Decreases

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Thanks to Novjot Chhabra

THE PROBLEM IS RC - HOW FAR CAN YOU GO?

A Theoretical Ideal

Aluminum (alloy) >>> Copper,			R reduction of
Resistivity	3.2	1.8	1.8 x

SiO2 >>>>>>>>>>> Air,			C reduction of
Dielectric Constant	4.2	1.0	4.2 x

RC Reduction of

7.5

Thanks to Novjot Chhabra

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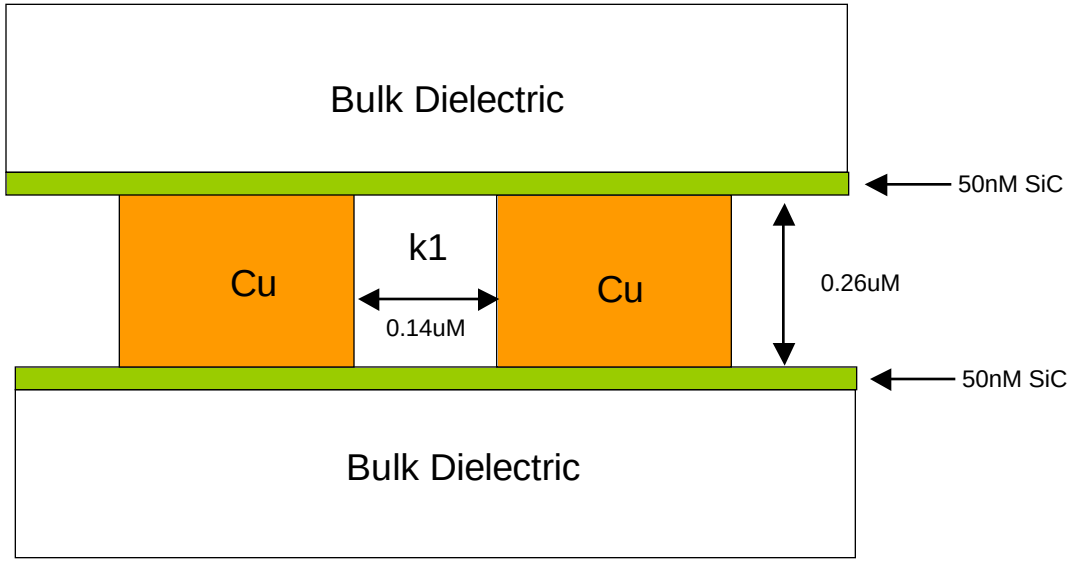
MODELED EFFECTIVE DIELECTRIC CONSTANTS



If bulk dielectric = 2.6 (SiLK*) then k_{eff} = 2.94
If bulk dielectric = 2.2 then k_{eff} = 2.57
If bulk dielectric = 1.5 then k_{eff} = 1.96
If bulk dielectric = 1.0 (Air) then k_{eff} = 1.5

* SiLK Semiconductor Dielectric, Trademark of the Dow Chemical Company

Thanks to Novjot Chhabra

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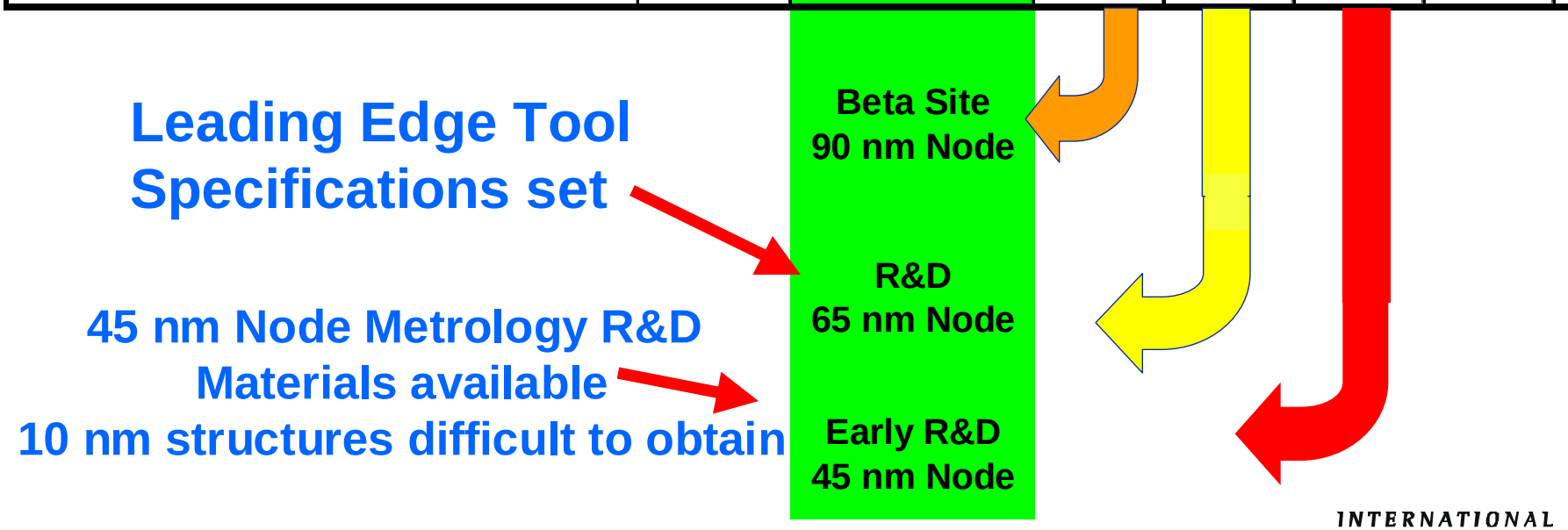
ITRS Challenge

	2001	2002	2004	2007	2010	2013	2016
Leading Production Technology Node = DRAM ½ Pitch	*130 nm*	*115 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*
MPU / ASIC ½ Pitch (nm)	150	130	90	65	45	32	22
MPU Printed Gate Length (nm)	90	75	53	35	25	18	13
MPU Physical Gate Length (nm)	65	53	37	25	18	13	9



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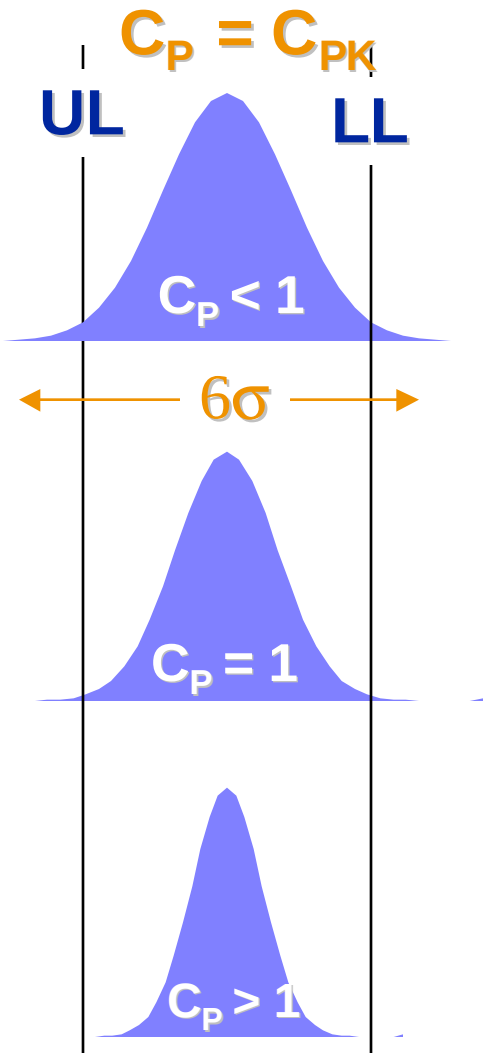
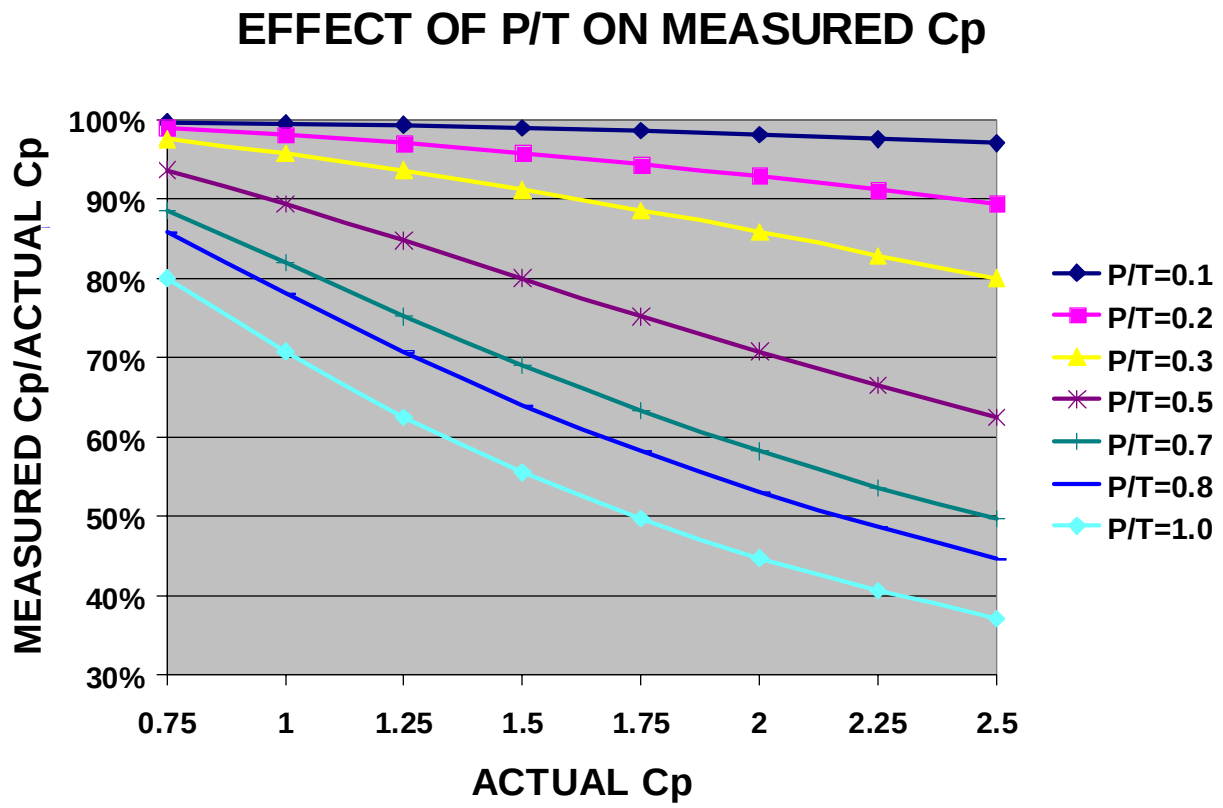
Process control
Is based on Statistical Significance





If Distribution is Centered

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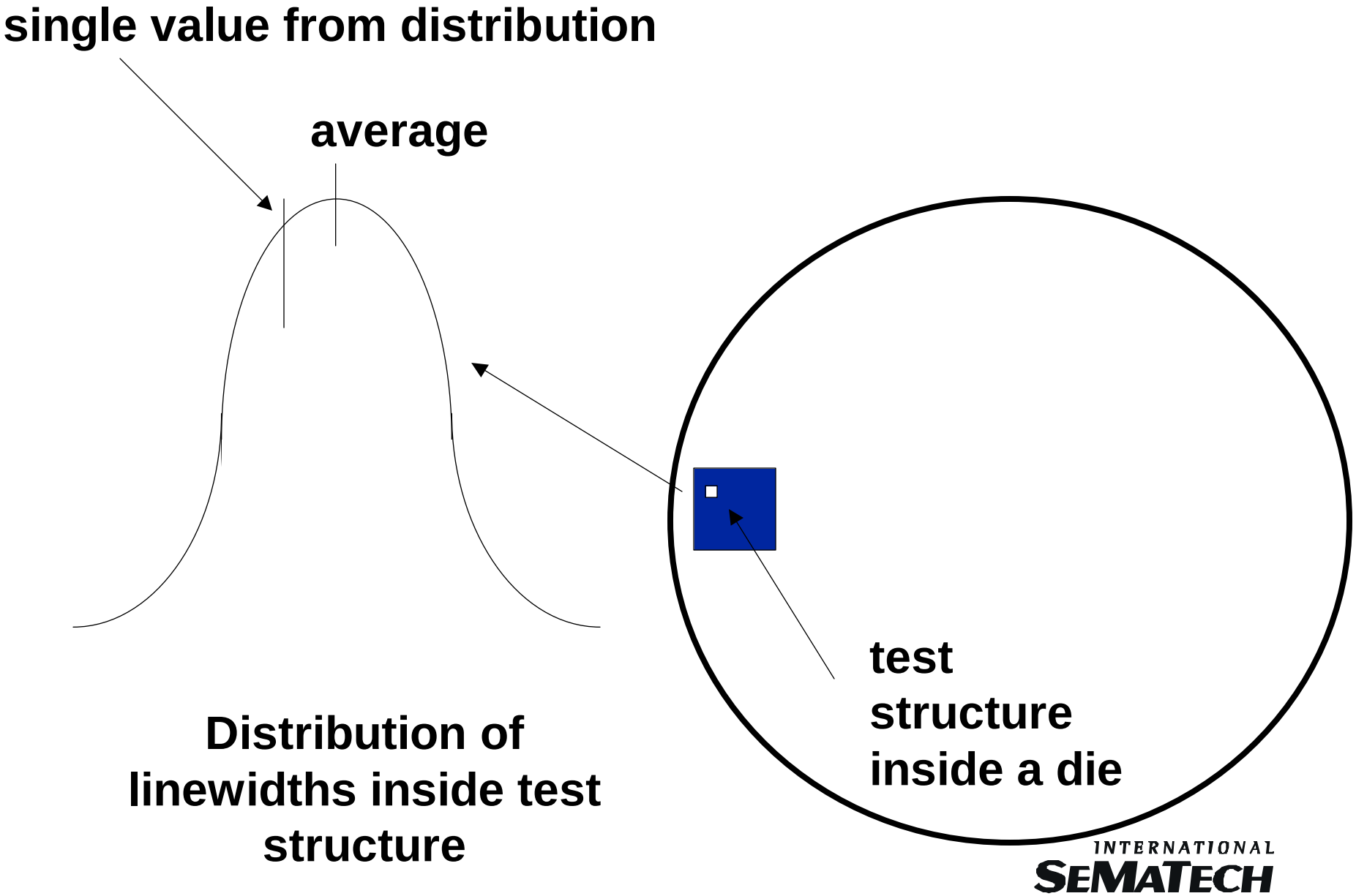
What are you Measuring?



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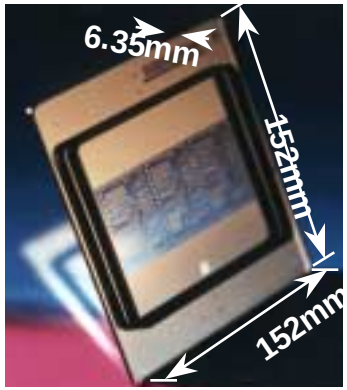
Litho Process and Metrology

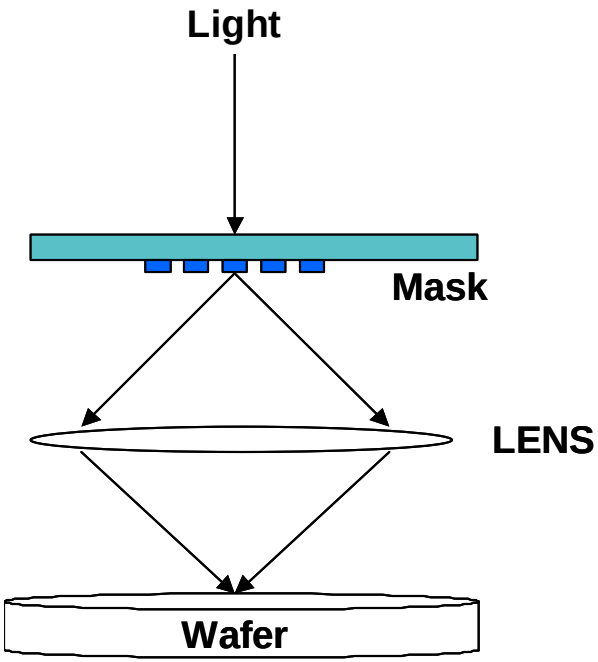
22 nm Node - 2016

CD Control Starts at the Mask



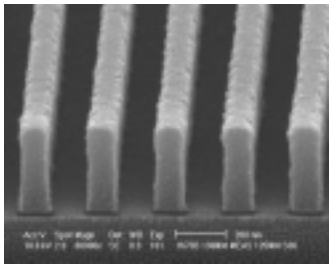
52 nm mask line width
26 nm scattering bars

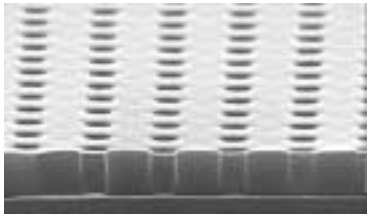
Overlay and CD Control after Exposure



13 nm printed line width

CD Control after Etch





9 nm physical line width

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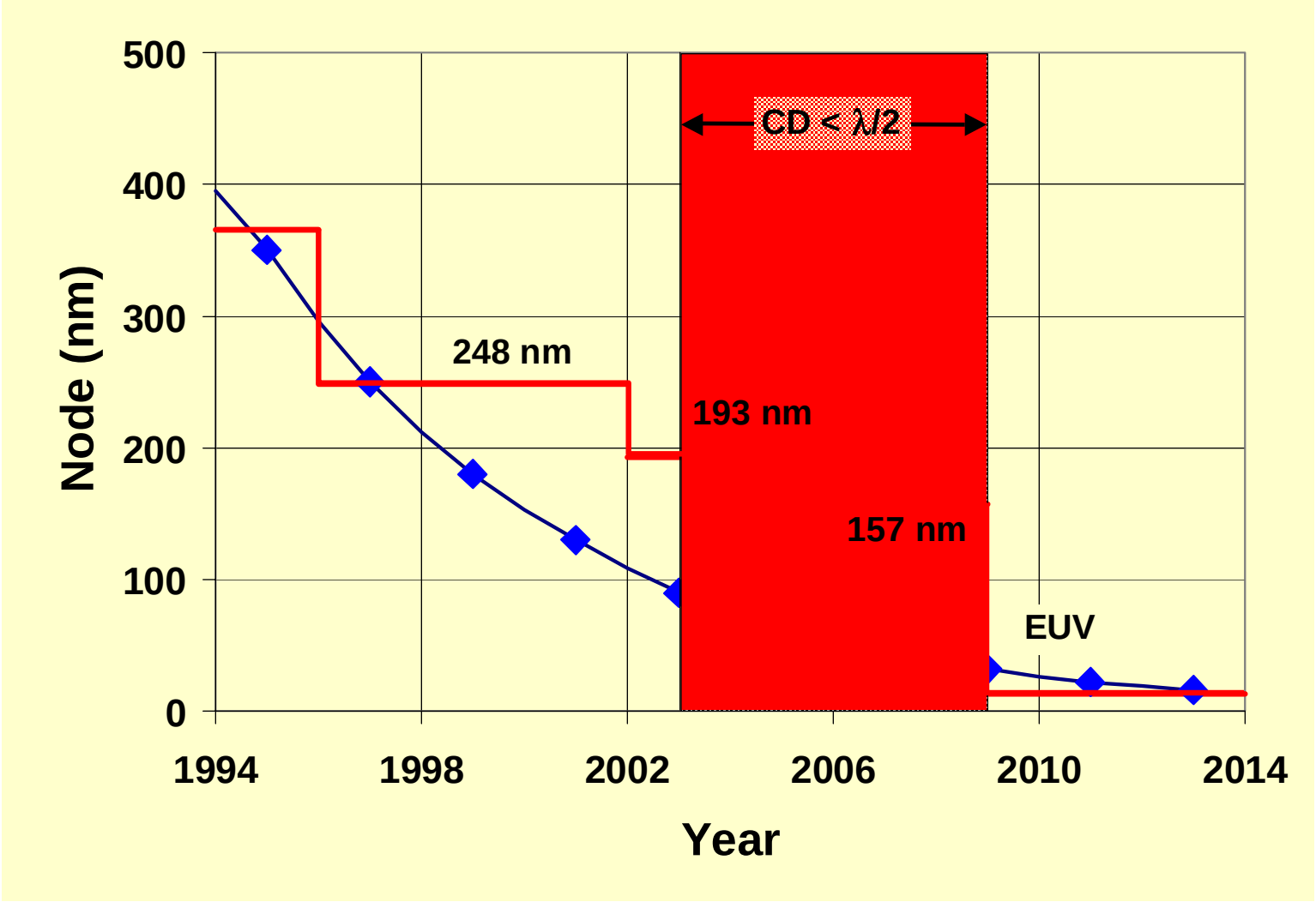
Optical Lithography
Feature Size vs Wavelength



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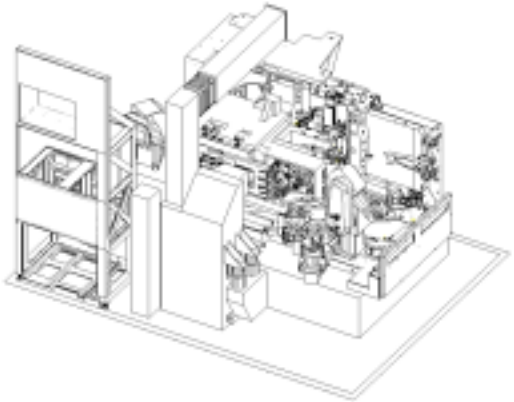
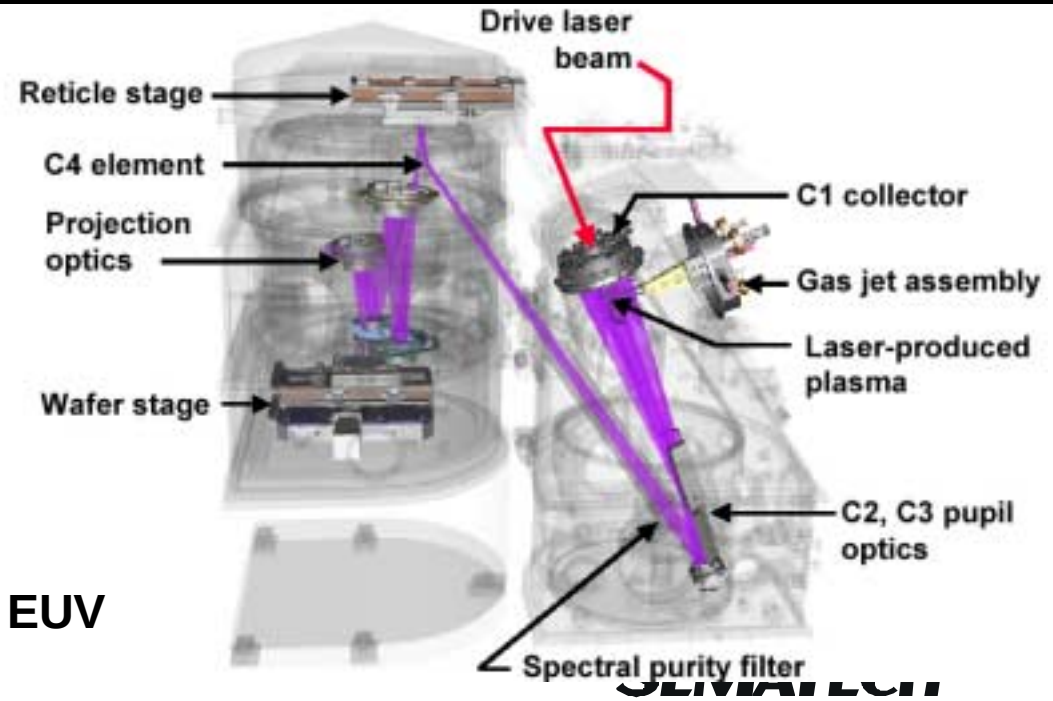
Litho Metrology

193 nm | 157 nm | EUV

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
Lithography Metrology							
Printed Gate CD Control (nm)	5.3	3	2	1.5	1.1	0.7	MPU
Wafer CD 3σ Precision P/T=0.2	1.1	0.6	0.4	0.3	0.2	0.1	MPU
Line Edge Roughness (nm)	4.5	2.7	1.8	1.3	0.9	0.65	MPU
Precision for LER	0.9	0.54	0.36	0.26	0.18	0.13	



193 and 157 nm



EUV

Physics of Resolution

- **Resolution $W = k \lambda/NA$**
- **To print small features use smaller the wavelengths**
- **Use tricks to Print features sizes close to the wavelength**

λ is the wavelength of the light

NA is the numerical aperture

NA = $\eta \sin\theta$ η is index of refraction

K is a constant that depends on the process

See Principles of Lithography, H. Levinson, p 19

Physics of Depth of Focus

- DoF $= k_2 \lambda / (NA)^2$ $\lambda >>$ feature size
- To print small features use smaller the wavelengths
- Use tricks to Print features sizes close to the wavelength

λ is the wavelength of the light

NA is the numerical aperture

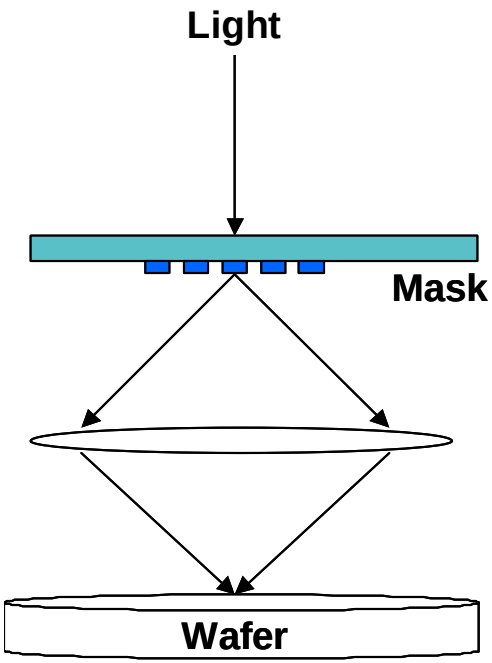
NA = $\eta \sin\theta$ η is index of refraction

K is a constant that depends on the process

See The Rayleigh Depth of Focus, C. Mack, Microlithography World: Feb 2004

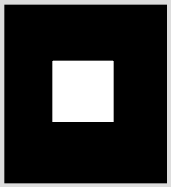
Tricks to extend Optical Lithography
Mask features that do not print

SIDE View

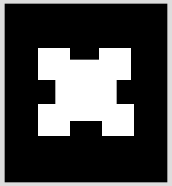


Optical Proximity Corrections

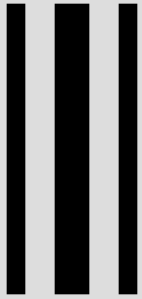
Contact



Contact W/ OPC



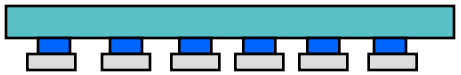
TOP View



Isolated Line w/ Scattering Bars

Phase Shift Masks

Alternating Phase Shift



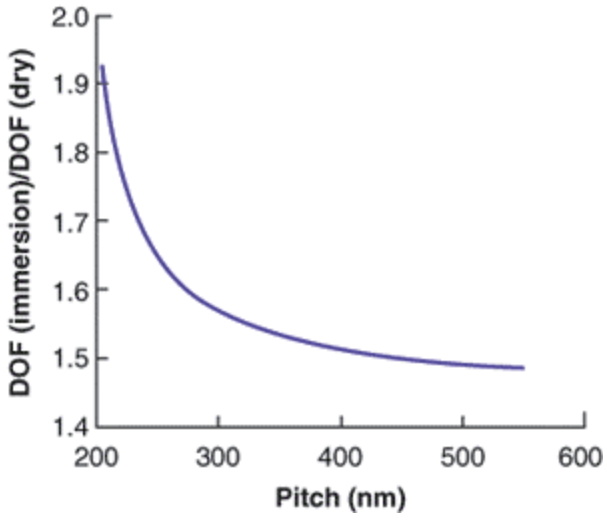
Rim Phase Shift

Many other types

INTERNATIONAL SEMATECH

Immersion LENS

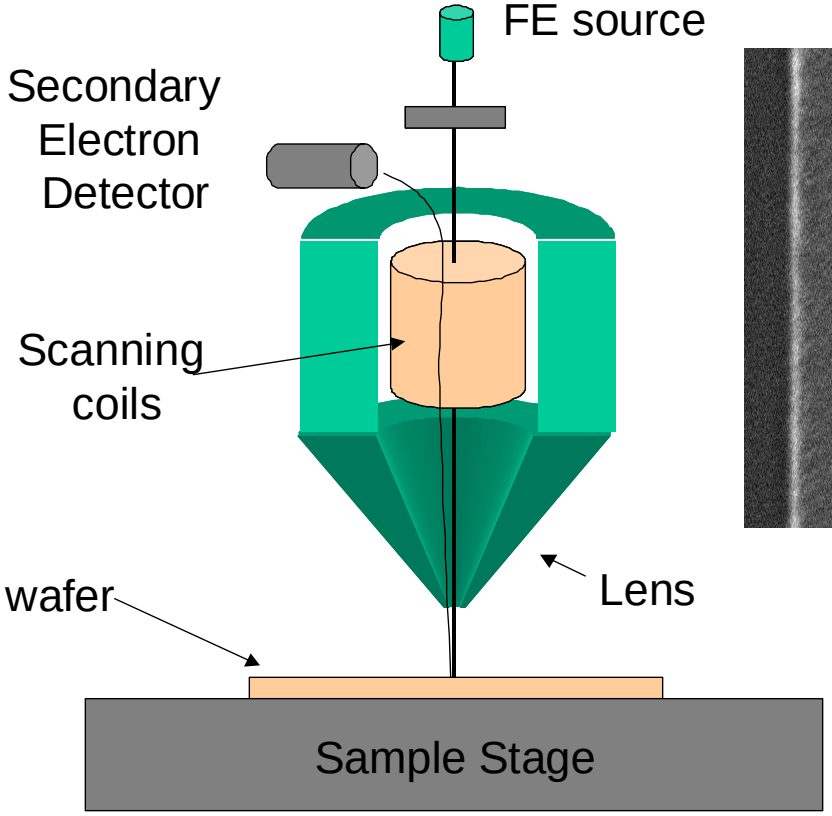
- **Change NA by changing refractive index from air η = 1 to water η = 1.46**
- **Extends 193 nm Litho to smaller feature sizes W(immersion)/W(dry) = 1/1.46 ~ 0.7**
- **DoF(immersion)/DoF (dry) at 193 nm**



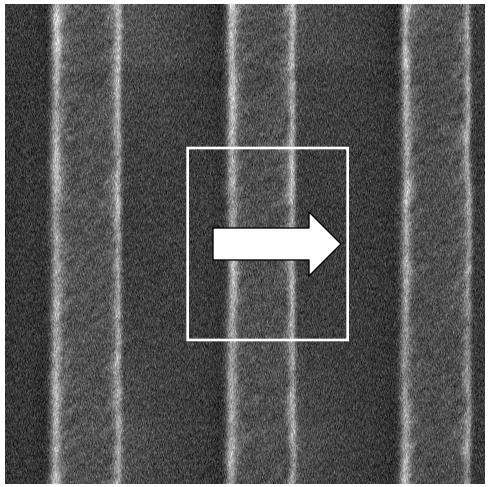
See The Rayleigh Depth of Focus, C. Mack, Microlithography World: Feb 2004

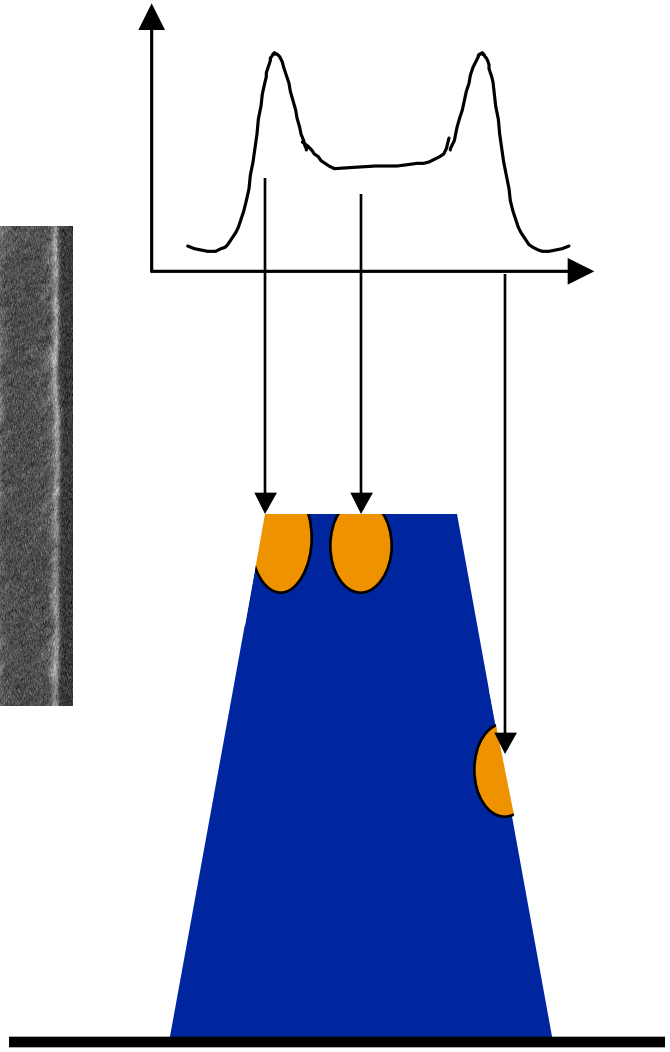
INTERNATIONAL SEMATECH

Low Energy SEM for CD Measurements



Top Down Image

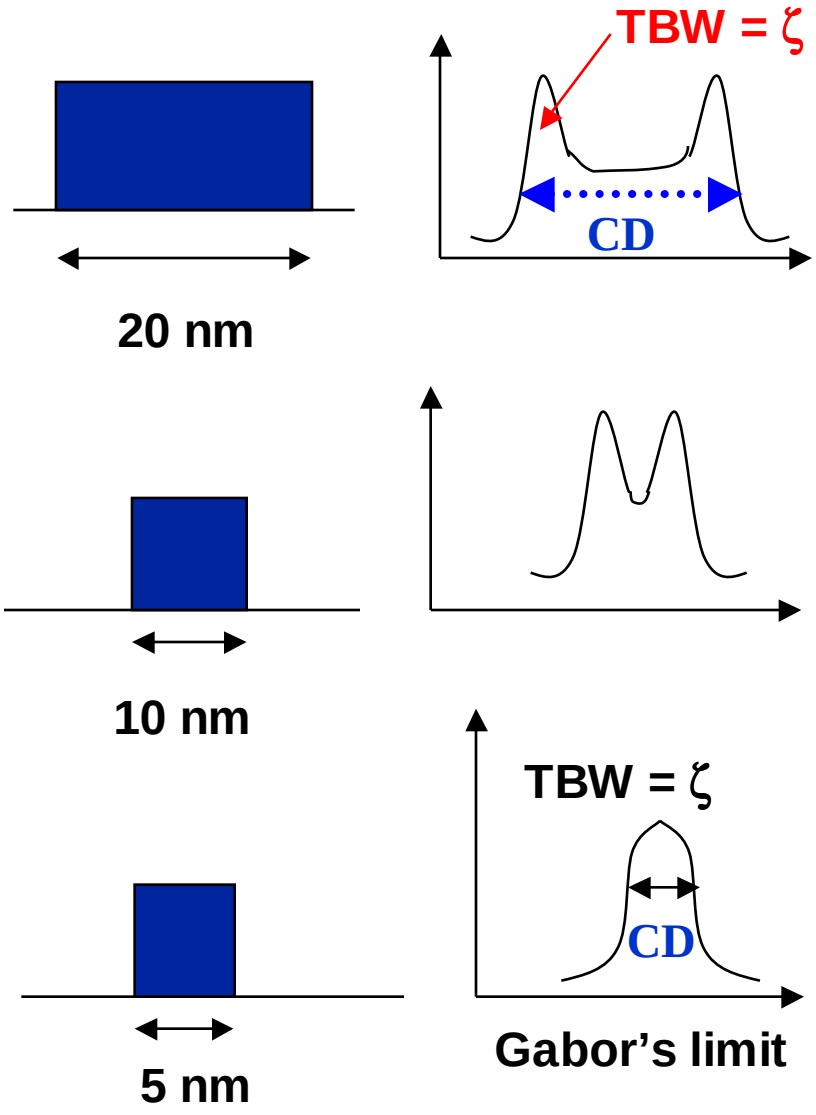




Thanks to David Joy

INTERNATIONAL SEMATECH

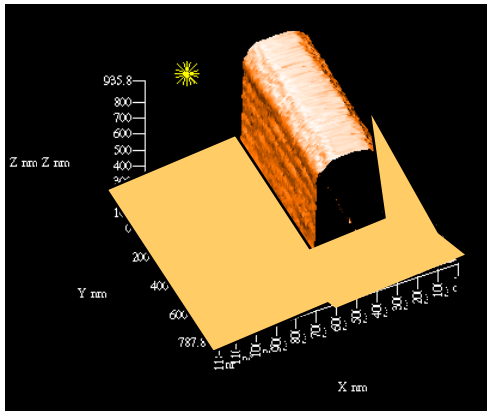
Limits of SEM for CD Measurements



Thanks to David Joy

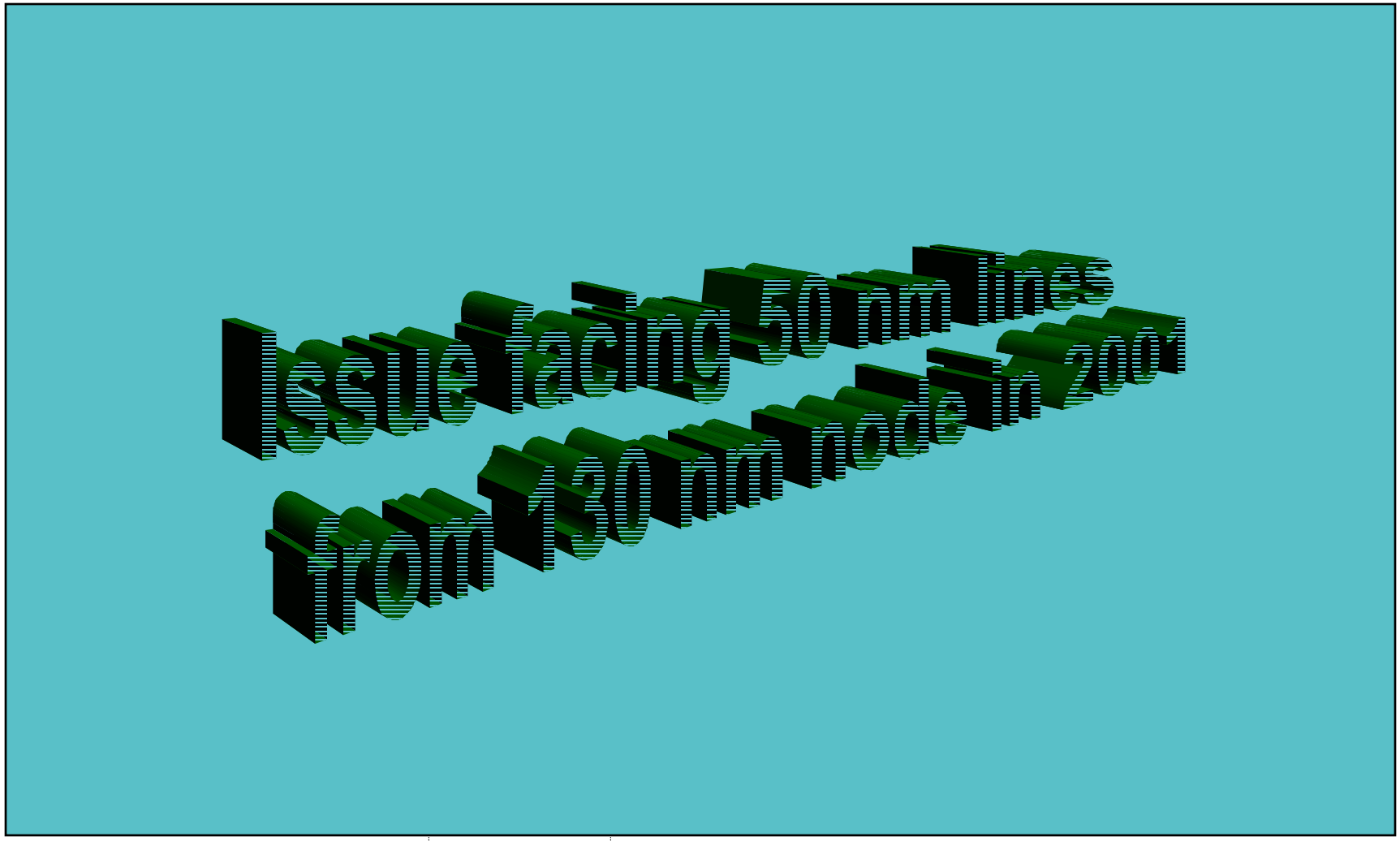
Loss of Depth of Field

DoF = (resolution)/(convergence angle)



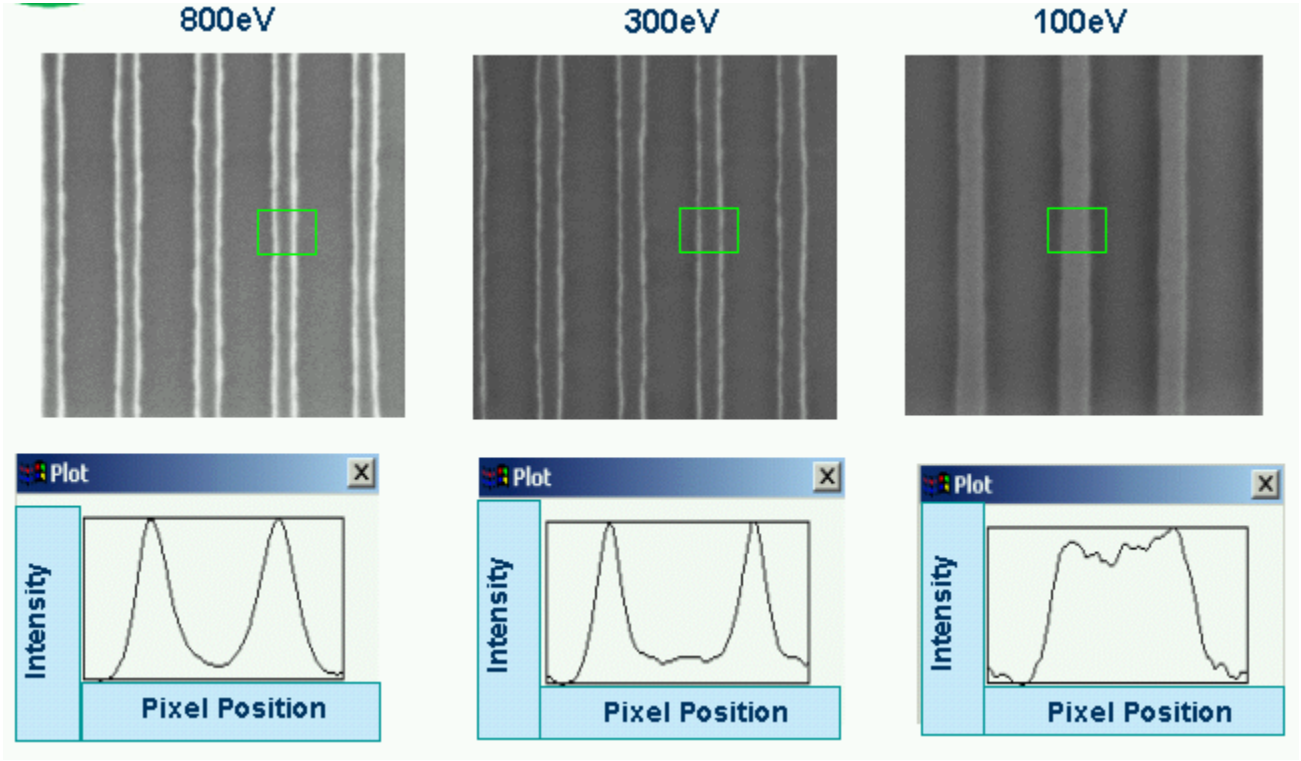
INTERNATIONAL SEMATECH

Challenges: Round Top Resist & LER



INTERNATIONAL SEMATECH

Ultra Low Voltage CD-SEM



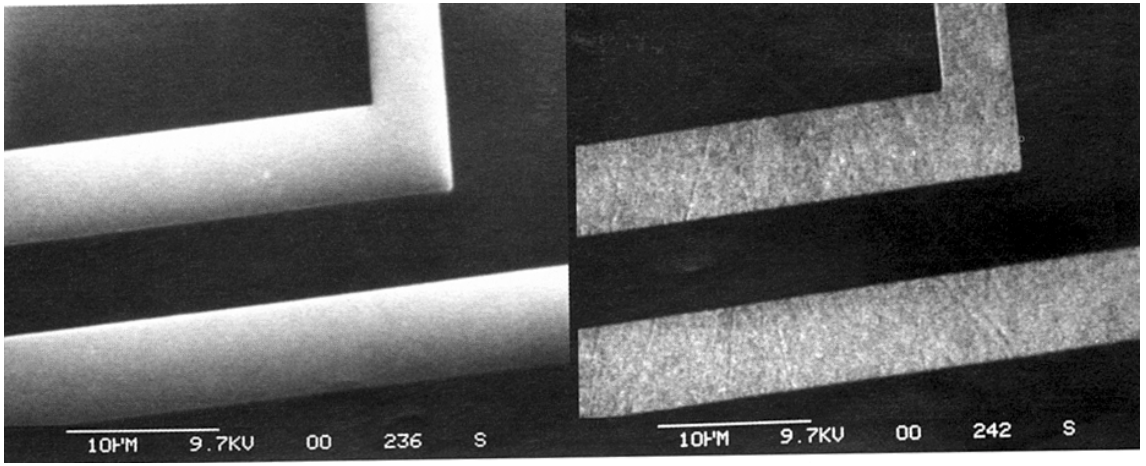
Thanks to Neal Sullivan of Schlumberger

INTERNATIONAL SEMATECH

Lithography CD Metrology

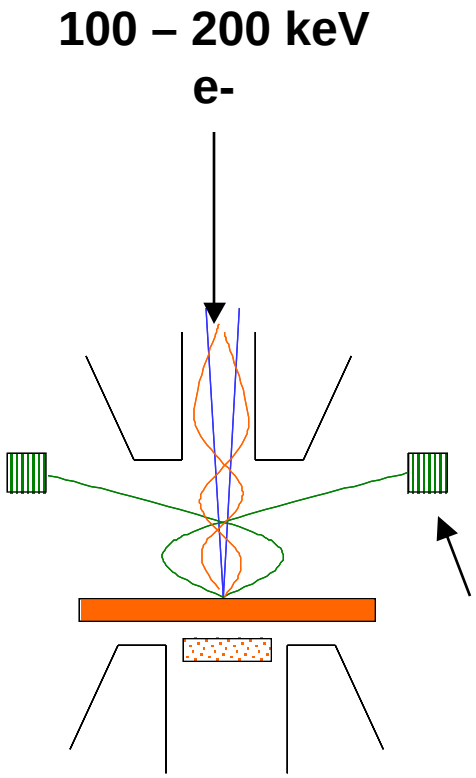
Improve CD-SEM thru 65 nm node

High Voltage CD-SEM



Comparison of conventional SE (left) and Low Loss (right) images of copper interconnects. Note the greatly enhanced surface detail and lack of edge brightness in the Low Loss image.

Micrograph courtesy of O C Wells

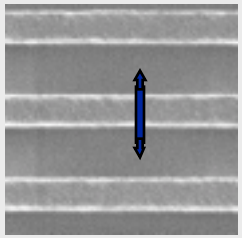


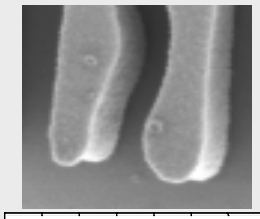
Figures from David Joy

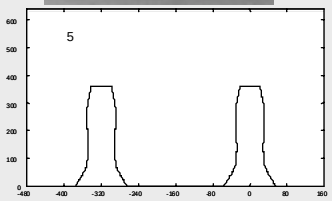
INTERNATIONAL SEMATECH

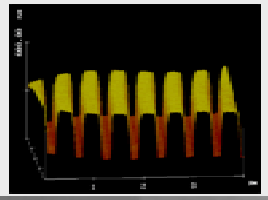
3D CD Metrology

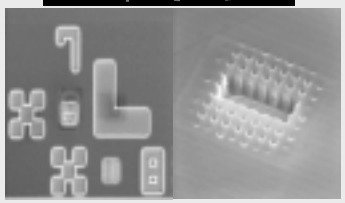
SEM – Scatterometry – CD-AFM











Commercially available

Software comparison of top down line scan of edge to golden image

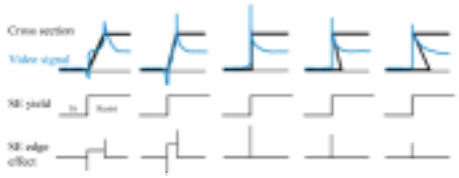
Tilt Beam SEM

Scatterometry

CD-AFM

Dual Beam FIB (destructive)

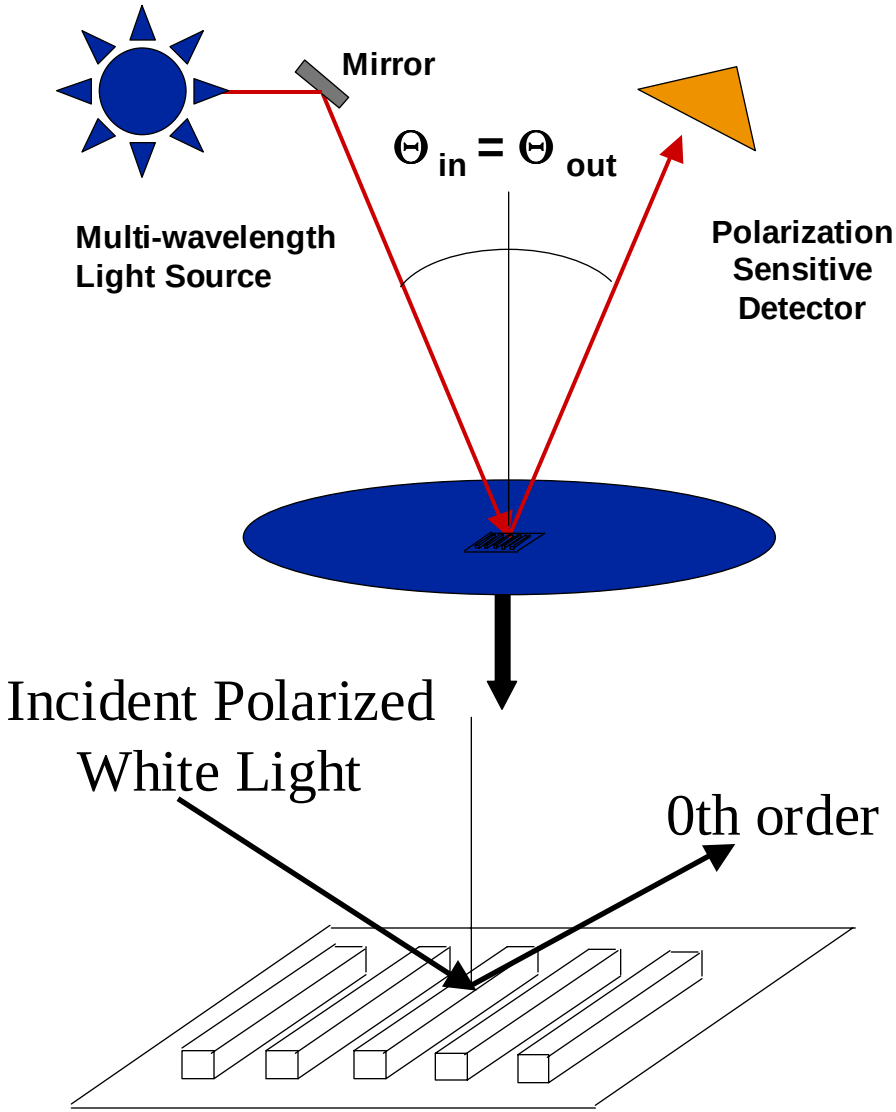
R&D



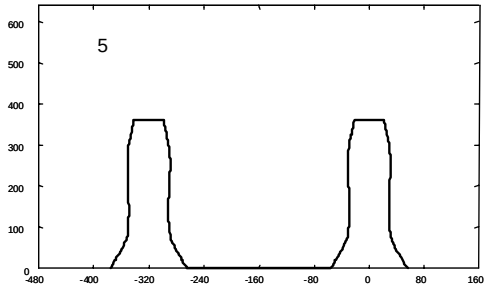
Software to convert top down image to 3D image

INTERNATIONAL SEMATECH

Scatterometry for CD Measurements



Real Time Calculation of line width & shape Eliminates Libraries



INTERNATIONAL SEMATECH

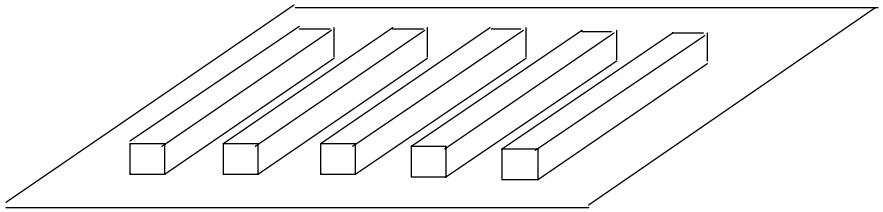
CD-AFM Limited by Probe Tip

Carbon Nanotube Probe tips

INTERNATIONAL SEMATECH

Average vs Individual

- CD-SEM measures one line at a time
- Scatterometry gives an average over many lines
- Reports indicate a large number (80 different lines) CD-SEM measurements in test area required to match scatterometry average
- Lose individual line information

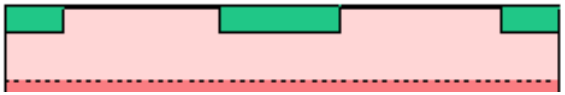


AGENDA

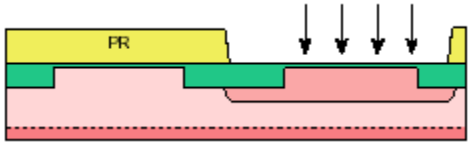
- The ITRS Challenge
- Litho Processes and Metrology
- FEP Processes and Metrology
- Interconnect Processes and Metrology
- Materials Characterization

Front End Processes & Metrology

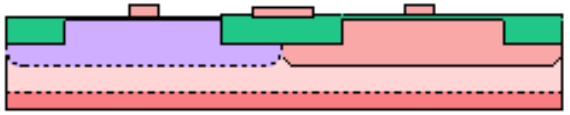
Shallow Trench Isolation



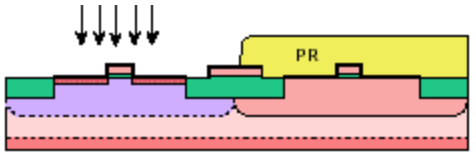
Pattern & Implant Wells



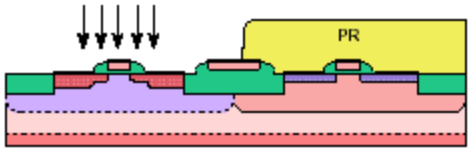
Pattern & Gate Dielectric

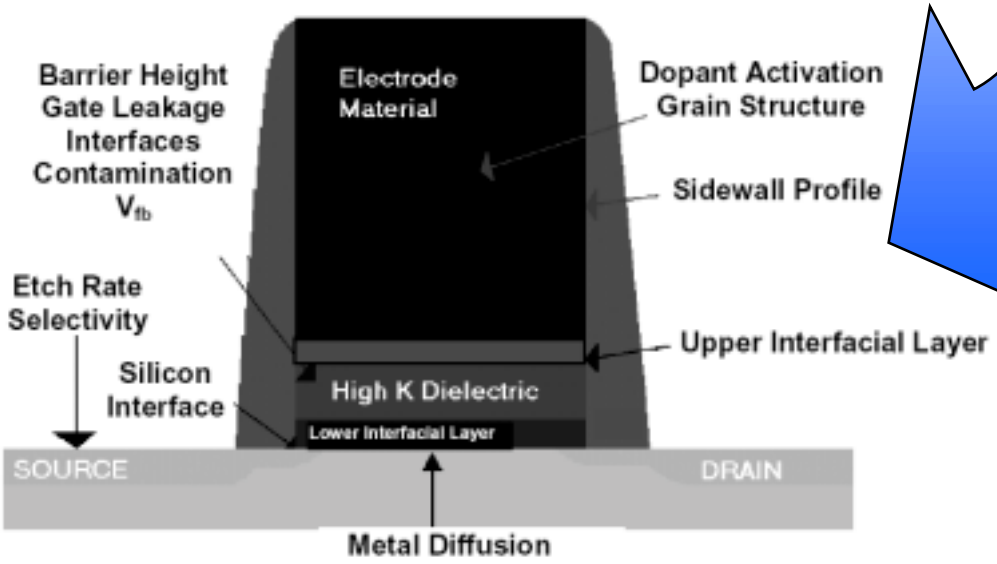


Pattern Poly/metal Implant LDD



Pattern & Implant S/D



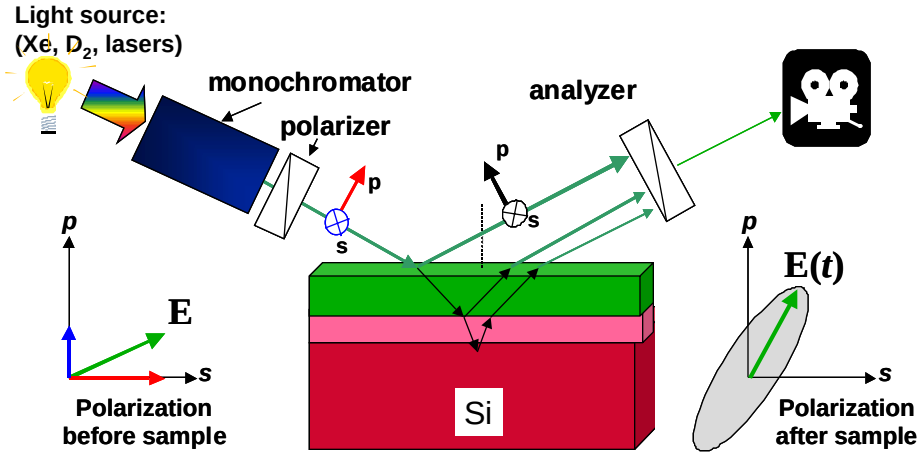


INTERNATIONAL SEMATECH

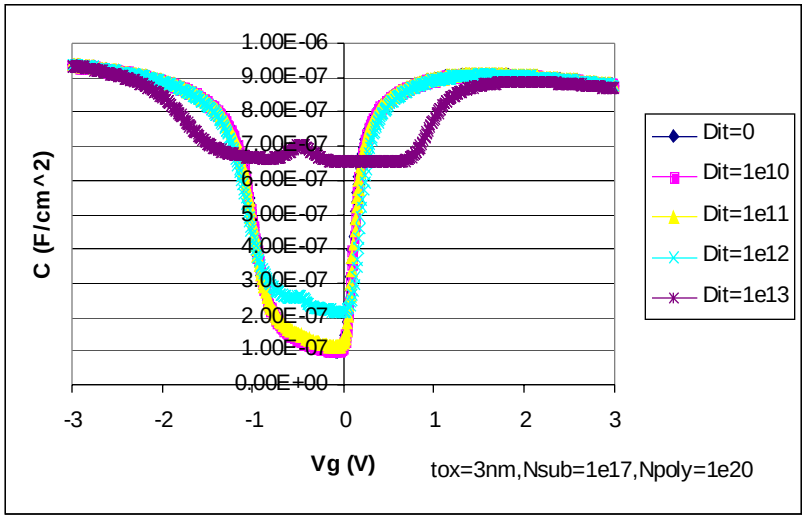
FEP : High κ Metrology

Technology Node	130 nm	90nm	65 nm	45 nm	32 nm	22 nm	Driver
Front End Processes Metrology							
High Performance Logic EOT equivalent oxide thickness (EOT) nm	1.3-1.6	0.9-1.4	0.6-1.1	0.5–0.8	0.4–0.6	0.4–0.5	MPU
Logic Dielectric EOT Precision 3σ (nm)	0.005	0.004	0.0024	0.0024	0.0016	0.0016	MPU
Metrology for Ultra-Shallow Junctions at Channel Xj (nm)	26	14.8	10	7.2	5.2	3.6	MPU

High κ near UV light absorption
Makes thin interfacial layer difficult to measure



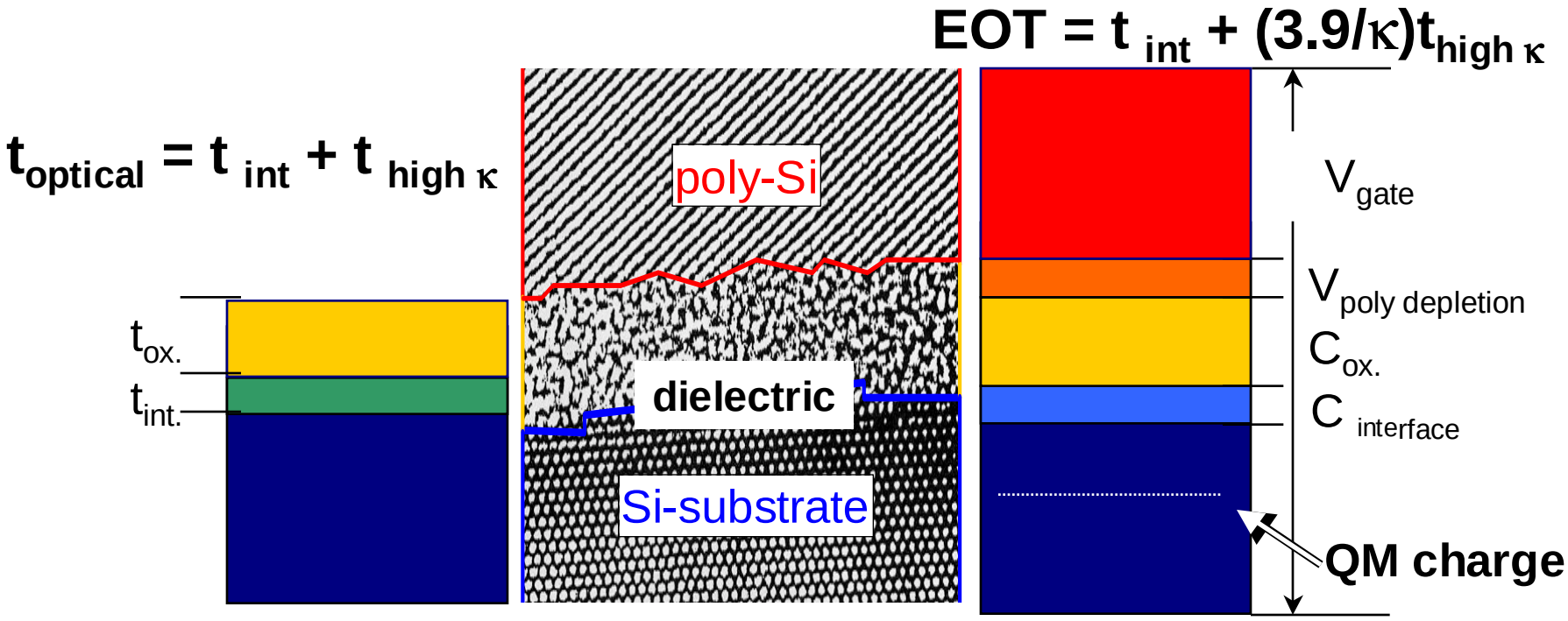
"Out of the Furnace"
High D_{it}
= Error in EOT



INTERNATIONAL SEMATECH

Optical/X-ray vs Electrical Measurement

C-V Structures receive Further Processing
Optical thickness vs electrical EOT
Capacitance of a very thin interface can have big effect



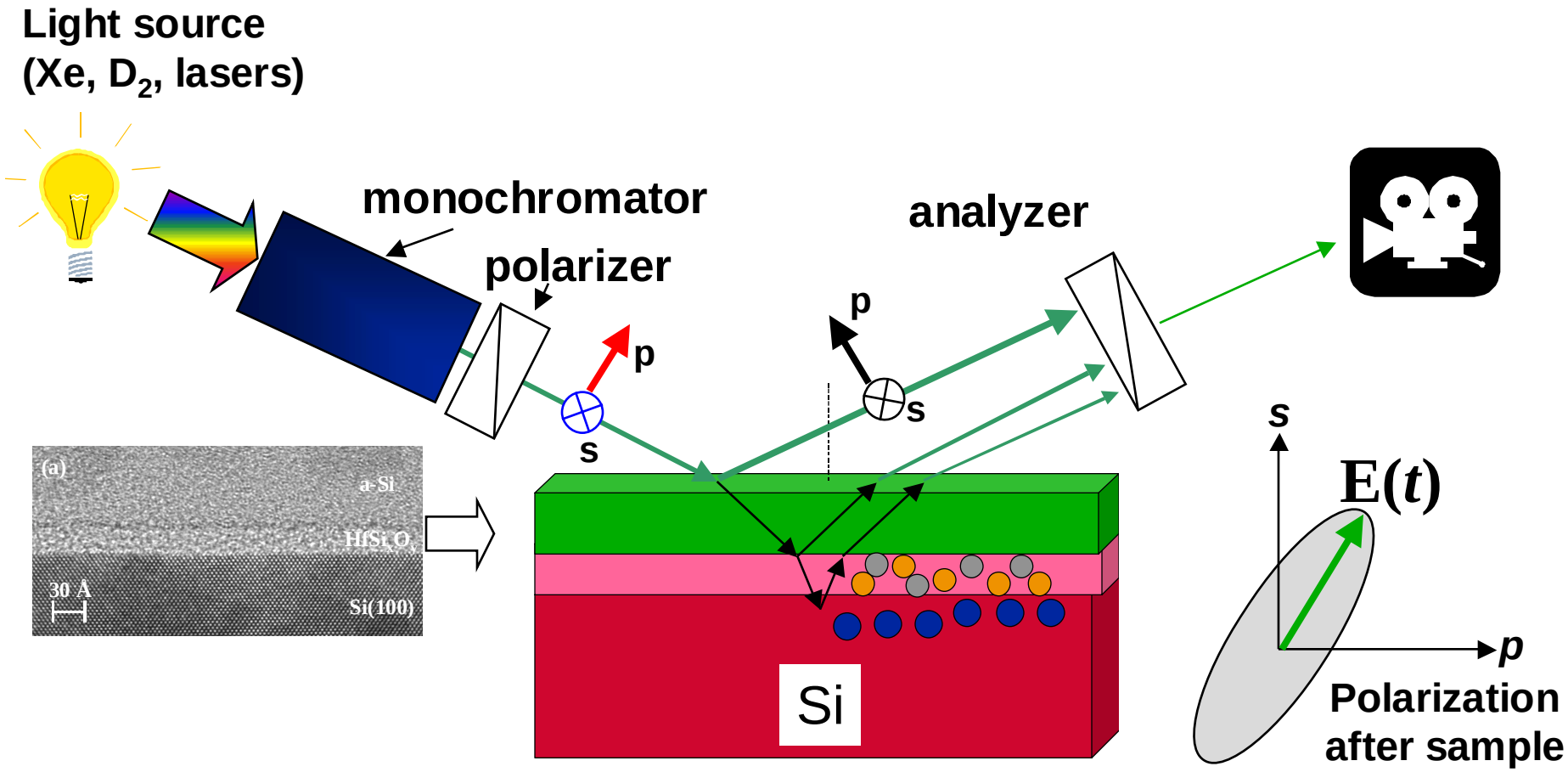
Optical ⟺ **Physical** ⟺ **Traditional Electrical**

(Process Monitoring) **(Performance/Reliability)**

See also : C Richter in Char & Met for ULSI 2000

INTERNATIONAL SEMATECH

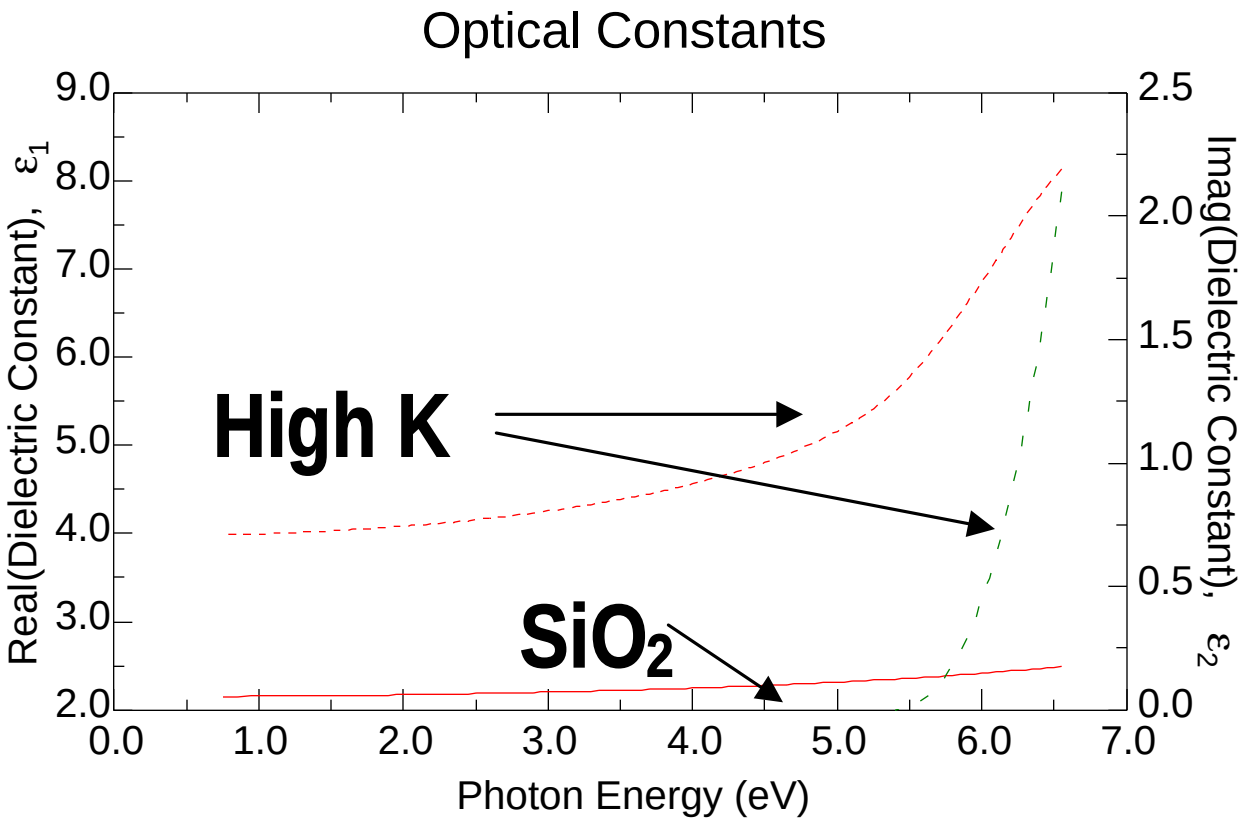
SPC requires measurement to Average Gate Dielectric over large area



2002 ALMC concensus method for TEM

INTERNATIONAL SEMATECH

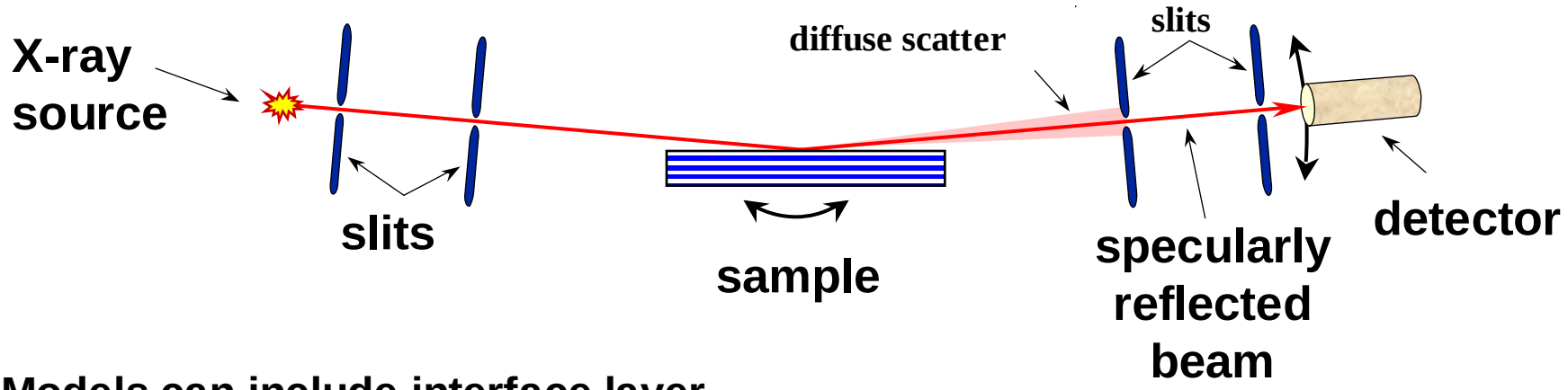
New Optical Models for higher κ



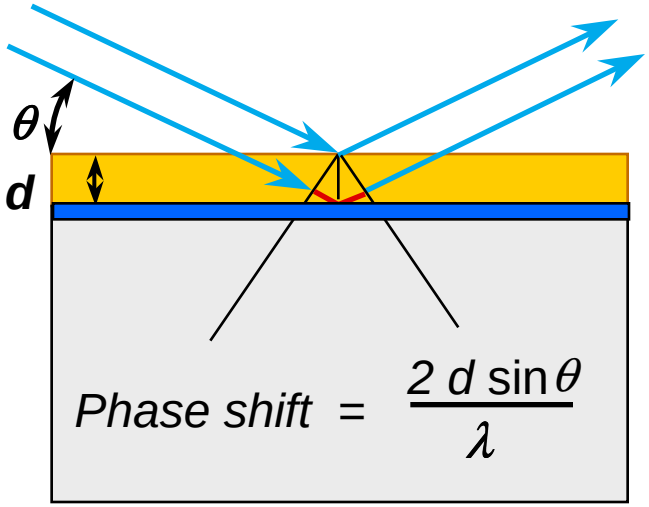
In-Line Metrology Suppliers continue to use older damped oscillator models

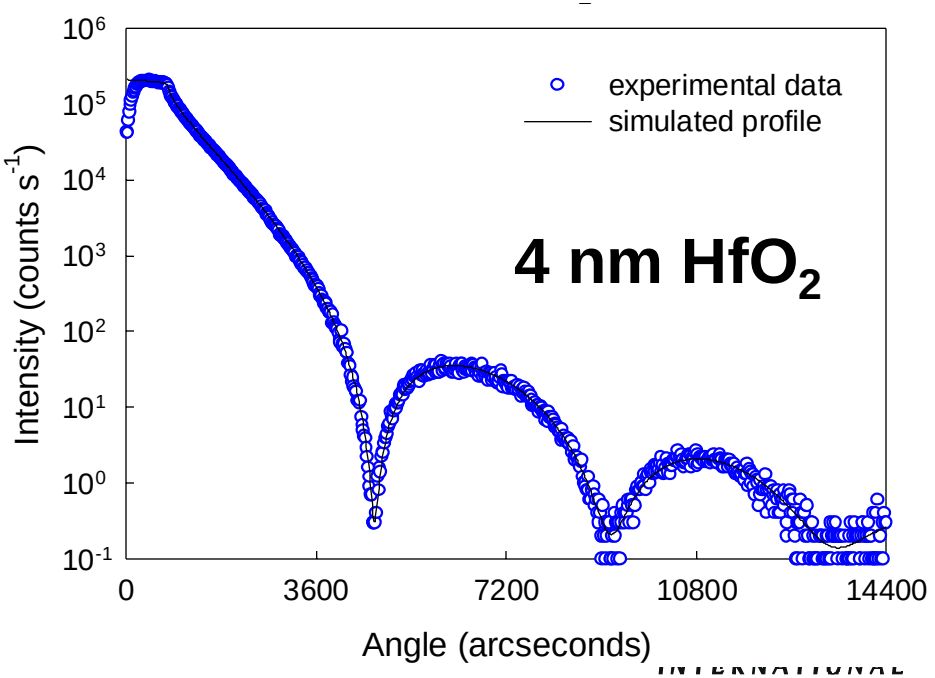
INTERNATIONAL SEMATECH

Simplified X-ray Path for X-ray reflectometer



Models can include interface layer

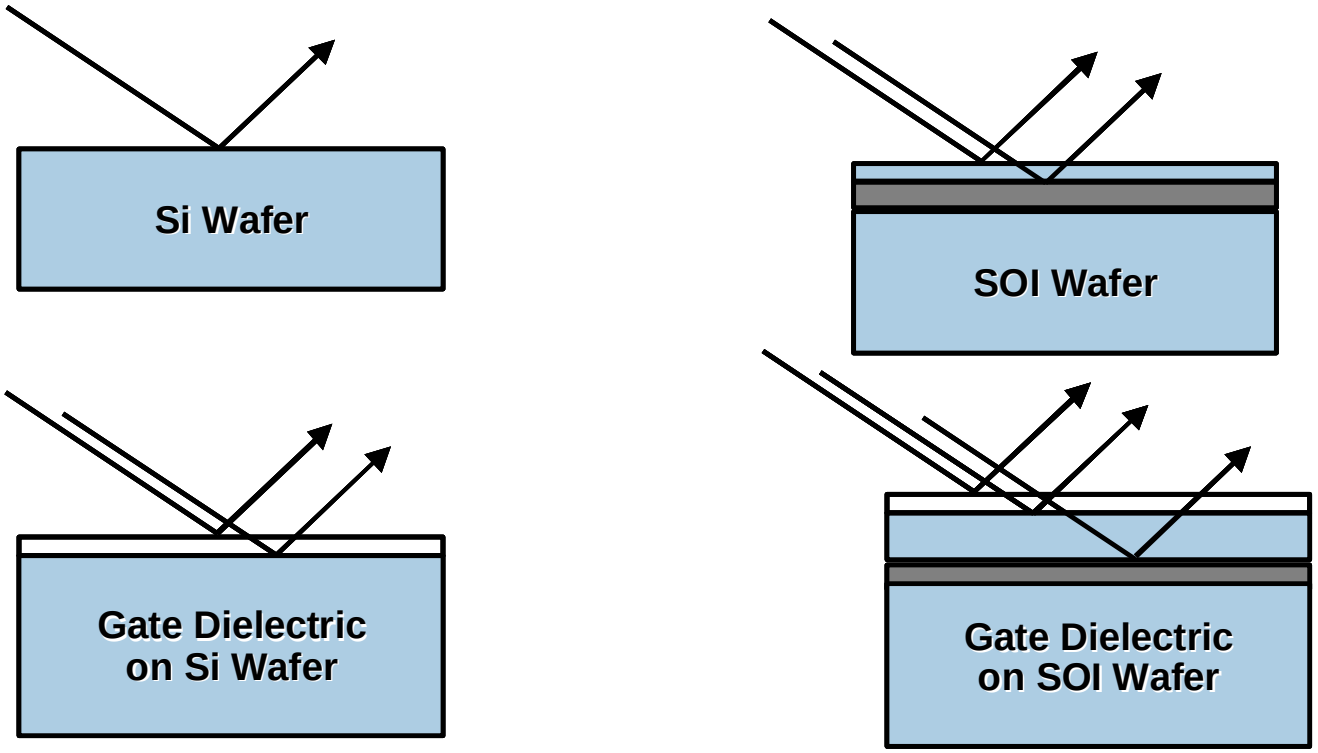




Thanks to Rich Matyi

INTERNATIONAL SEMATECH

Extra reflection from SOI Wafers Impacts Optical Measurements and Light Scattering



Quantum confinement for sub 20 nm silicon
Need SOI Optical Constants

INTERNATIONAL SEMATECH

AGENDA

- The ITRS Challenge
- Litho Processes and Metrology
- FEP Processes and Metrology
- Interconnect Processes and Metrology
- Materials Characterization

Interconnect Processes & Metrology

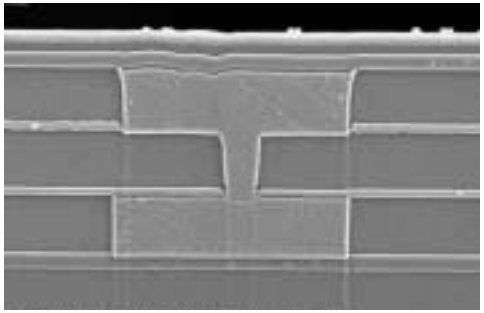
Pattern Low κ **Control Line width/depth and shape**

Deposit barrier and copper

Control barrier/copper & voiding

Chemical Mechanical Polishing

Control Flatness



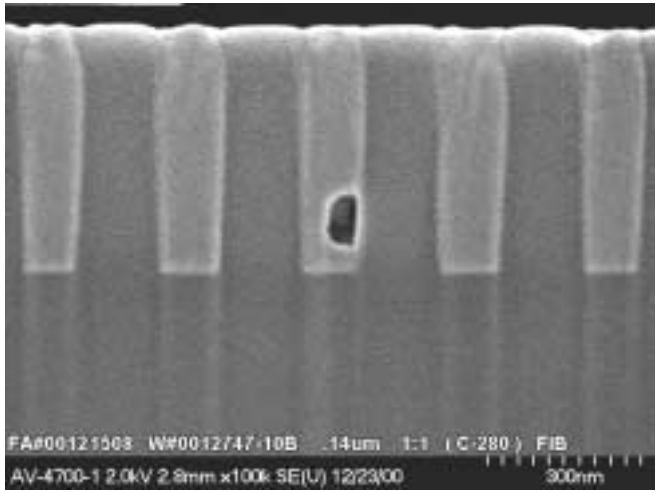
Low k / barrier
etch stop / low k

INTERNATIONAL SEMATECH

Gaps in Interconnect Metrology

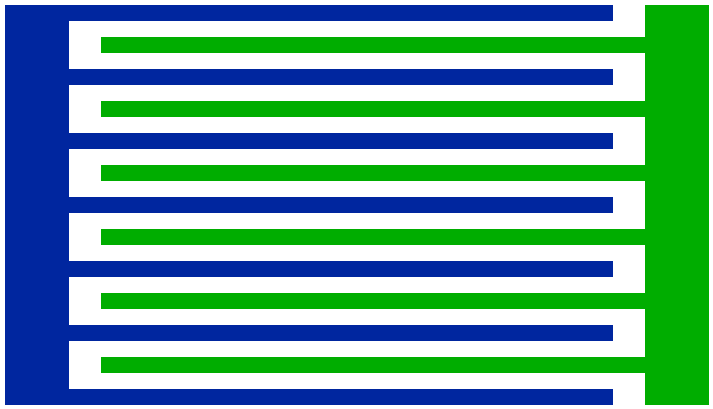
Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*
Interconnect Metrology						
Barrier layer thick (nm) process range (±3σ) Precision 1σ (nm)	**13 20% 0.04**	**10 20% 0.03**	**7 20% 0.02**	**5 20% 0.016**	**4 20% 0.013**	
Void Size for 1% Voiding in Cu Lines	**87**	**52**	**37**	**26**	**18**	**12**
Detection of Killer Pores at (nm) size	**6.5**	**4.5**	**3.25**	**2.25**	**1.6**	**1.1**

- **VOID Detection in Copper lines**
- **Killer Pore Detection in Low κ**
- **Barrier / Seed Cu on sidewalls**
- **Control of each new Low κ**



INTERNATIONAL SEMATECH

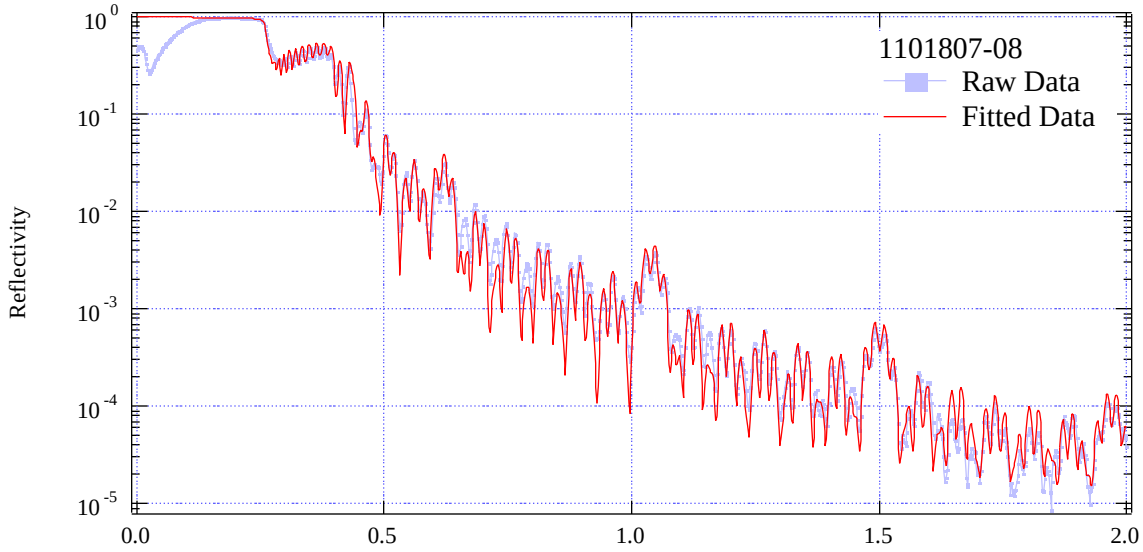
R-C test structures of new low κ Prior to manufacture

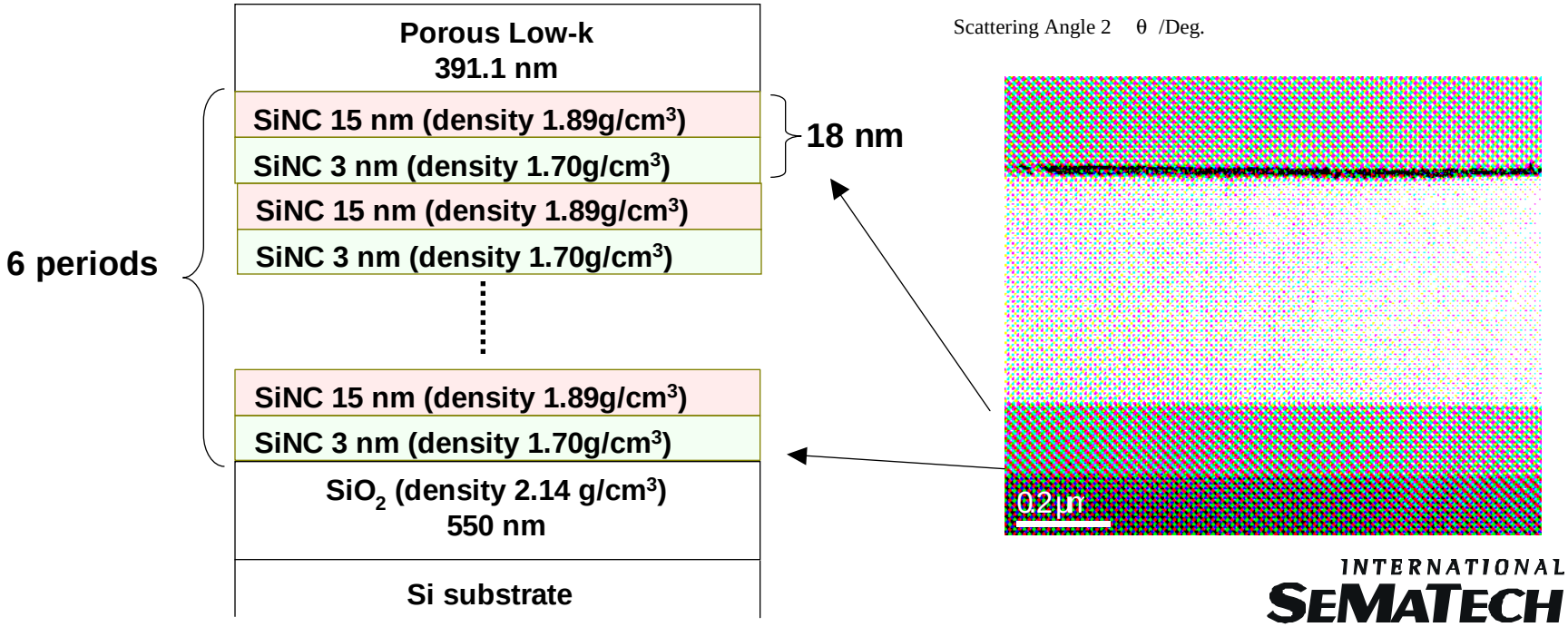


Capacitance Test

Resistance Test

XRR for low κ process control





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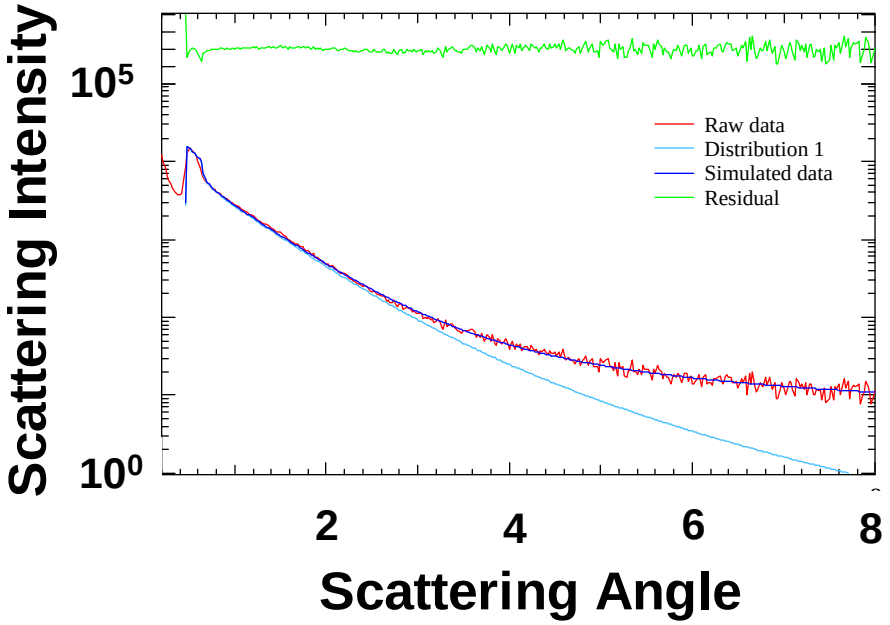
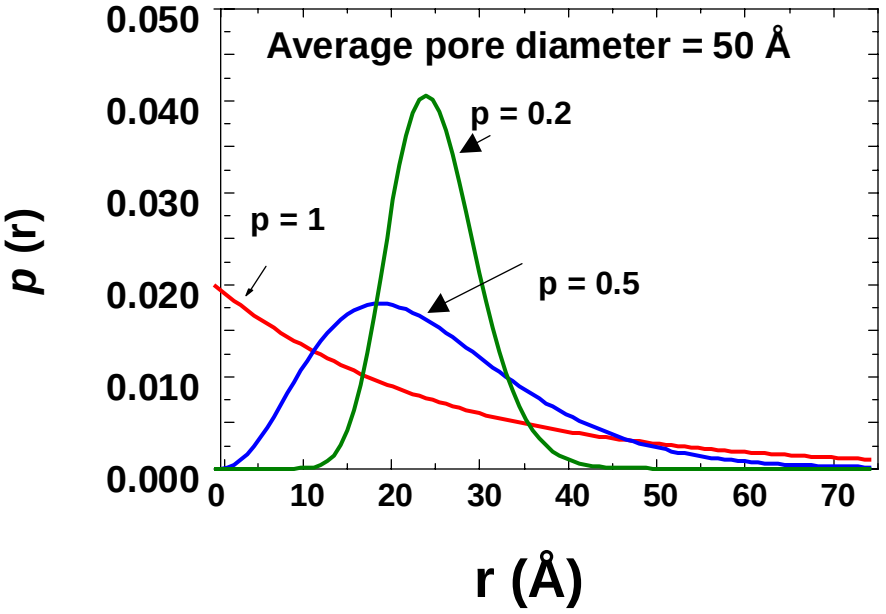
Pore Size Distribution
Diffuse (small angle) x-ray scattering





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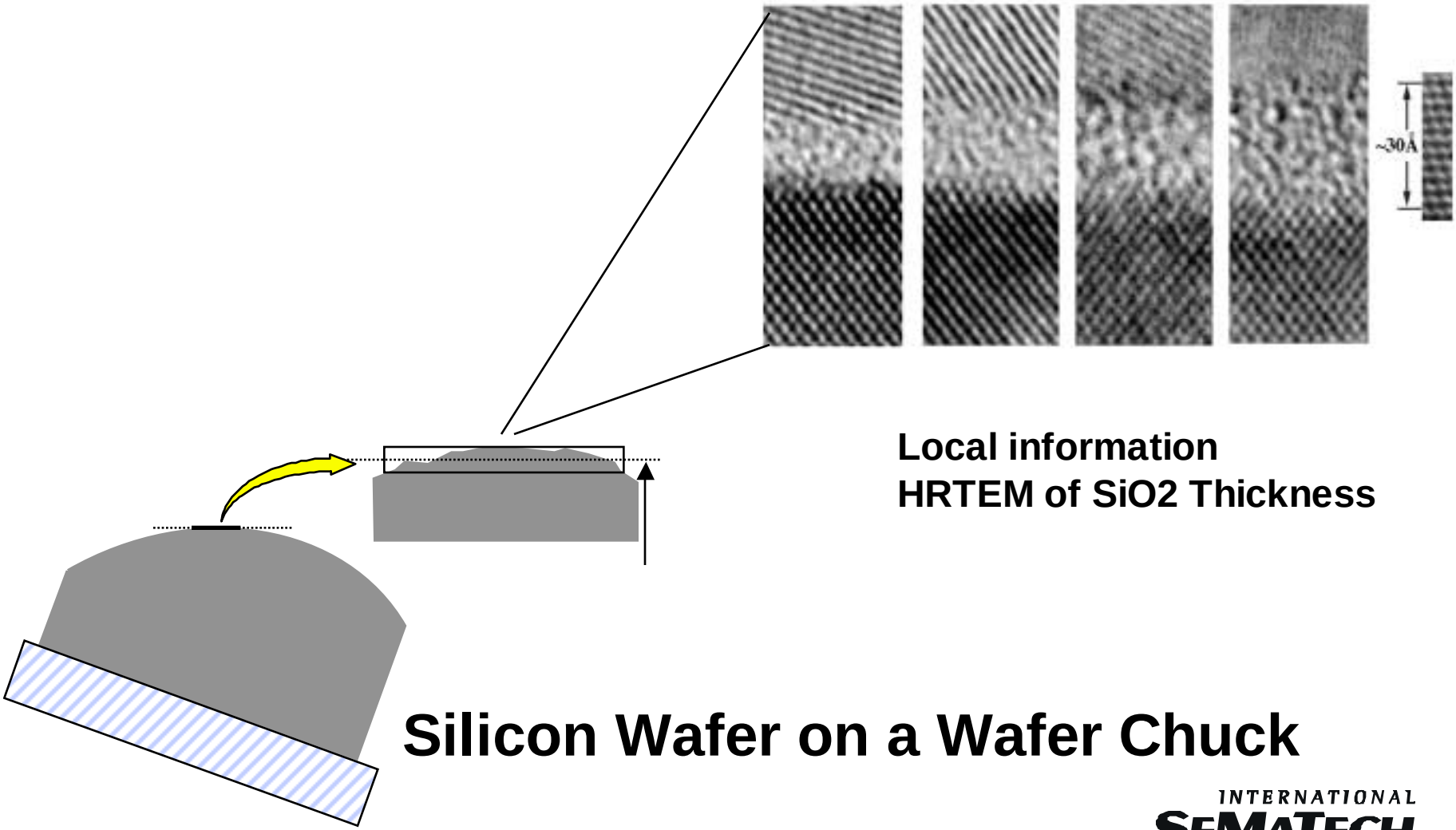
AGENDA

- The ITRS Challenge
- Litho Processes and Metrology
- FEP Processes and Metrology
- Interconnect Processes and Metrology
- Materials Characterization

Method Dependent Observation of Film Properties



Local information
HRTEM of SiO2 Thickness

Silicon Wafer on a Wafer Chuck

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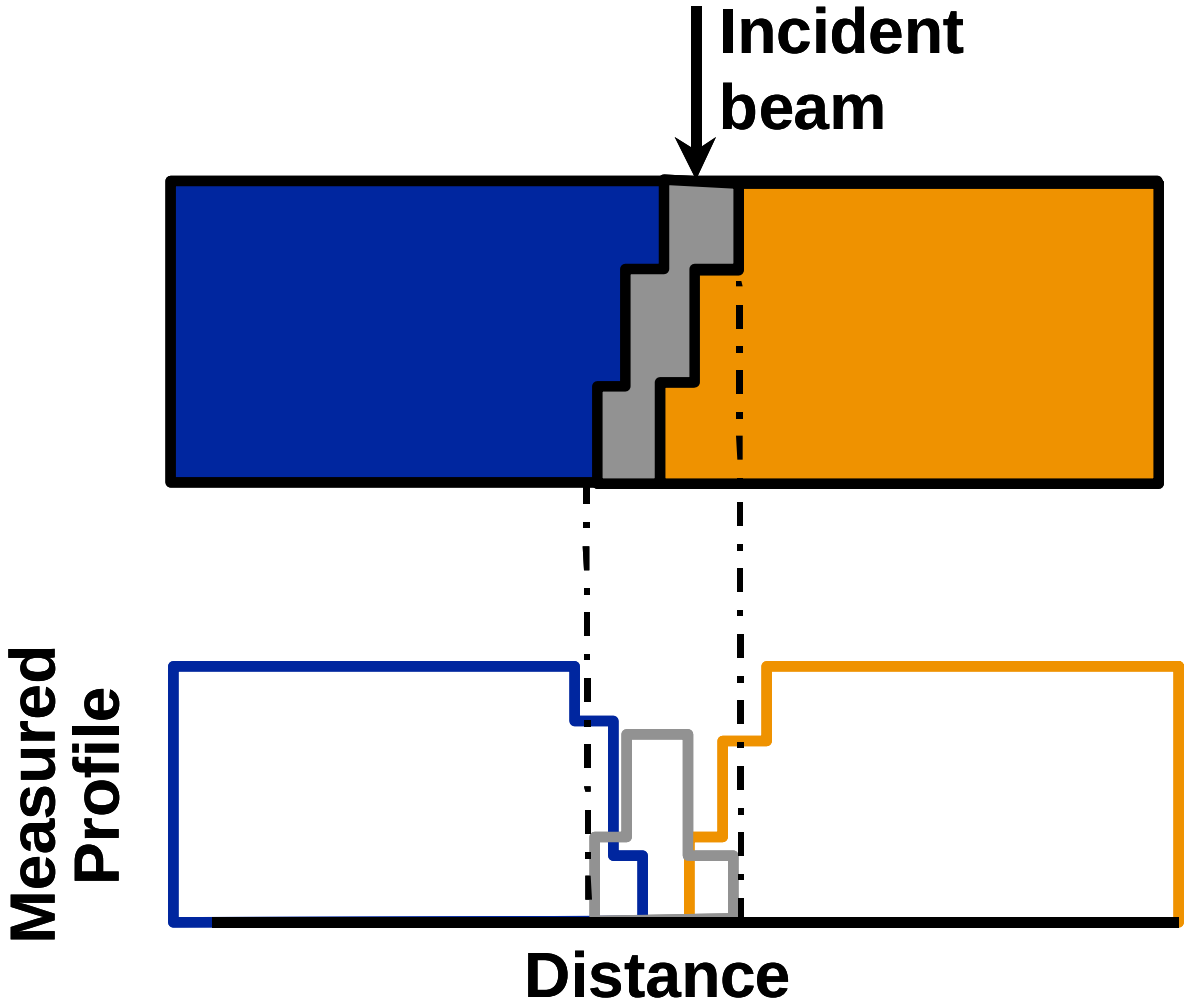
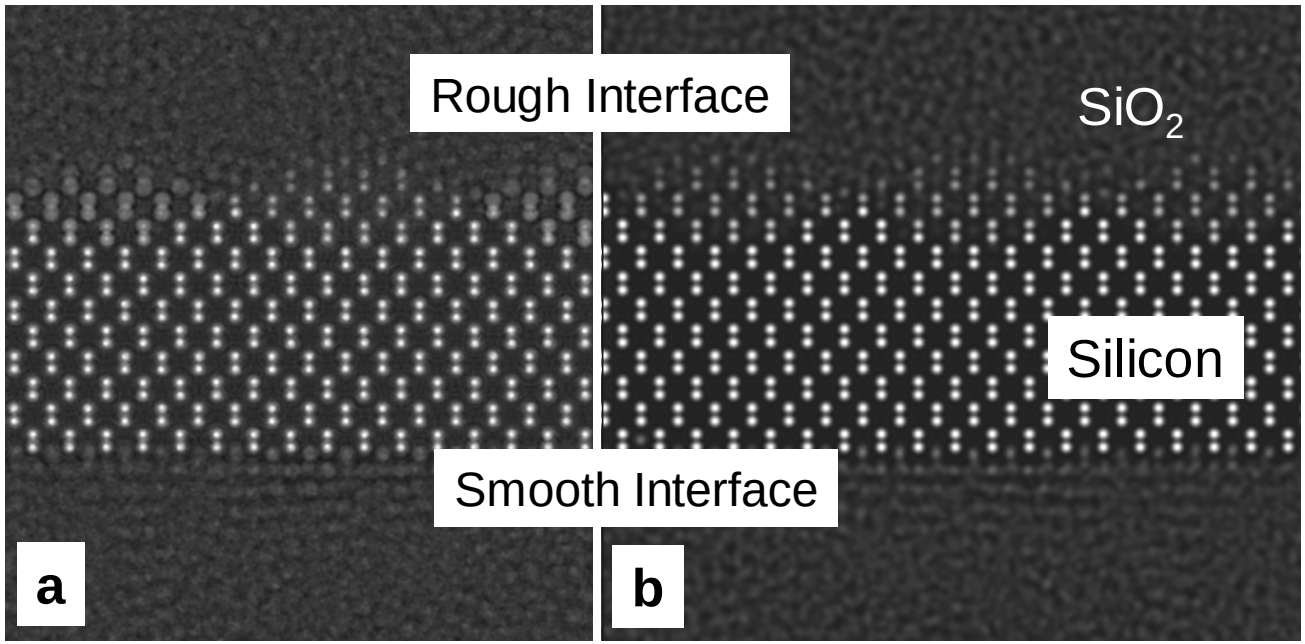
TEM Imaging of the Interface



TEM of thin gate dielectric

Simulation and Experimental Data show ADF-STEM and HR-TEM give same thickness



Consensus method uses 50 nm thick sample & ADF-STEM

Thanks to Dave Muller

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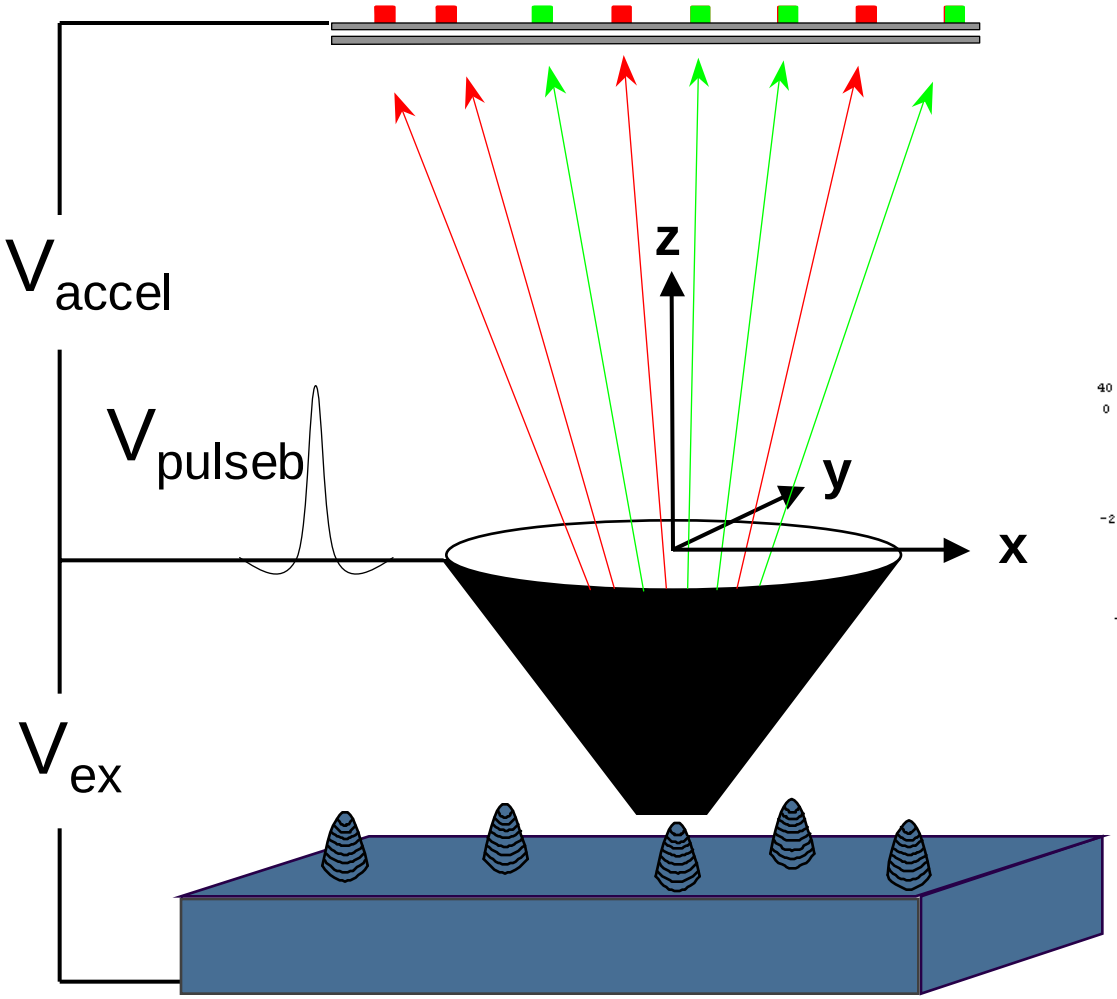
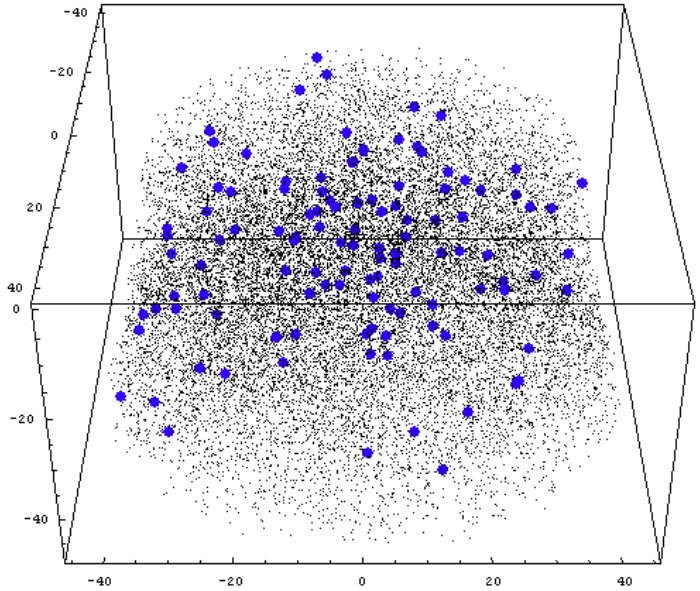
Local Electrode Atom Probe





Atom Distribution

: < 100% detection

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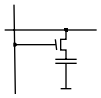
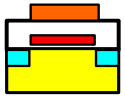
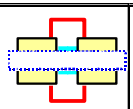
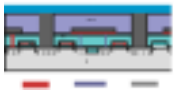
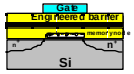
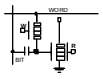
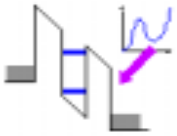
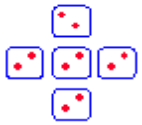
Metrology & New Structures

Memory

STORAGE MECHANISM	*BASELINE 2002 TECHNOLOGIES*		*MAGNETIC RAM*		*PHASE CHANGE MEMORY*	*NANO FLOATING GATE MEMORY*	*SINGLE/FEW ELECTRON MEMORIES*	*MOLECULAR MEMORIES*
								
DEVICE TYPES	*DRAM*	*NOR FLASH*	*PSEUDO-SPIN-VALVE*	*MAGNETIC TUNNEL JUNCTION*	*OUM*	*-ENGINEERED TUNNEL BARRIER -NANOCRYSTAL*	*SET*	*-BISTABLE SWITCH -MOLECULAR NEMS -SPIN BASED MOLECULAR DEVICES*

Logic

						
DEVICE	RESONANT TUNNELING DIODE – FET	SINGLE ELECTRON TRANSISTOR	RAPID SINGLE QUANTUM FLUX LOGIC	QUANTUM CELLULAR AUTOMATA	NANOTUBE DEVICES	MOLECULAR DEVICES
TYPES	**3-terminal**	**3-terminal**	**Josephson Junction +inductance loop**	**-Electronic QCA -Magnetic QCA**	**FET**	**2-terminal and 3-terminal**

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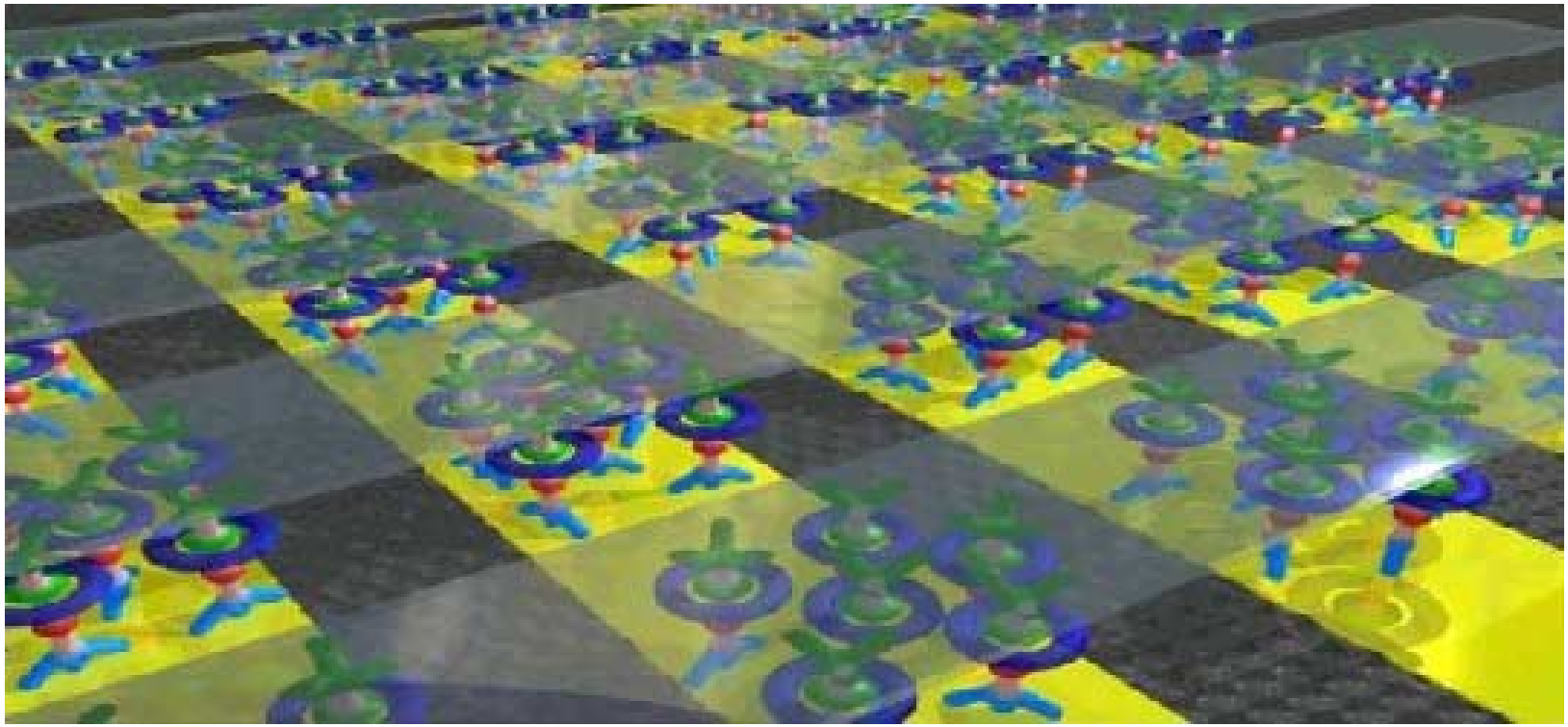
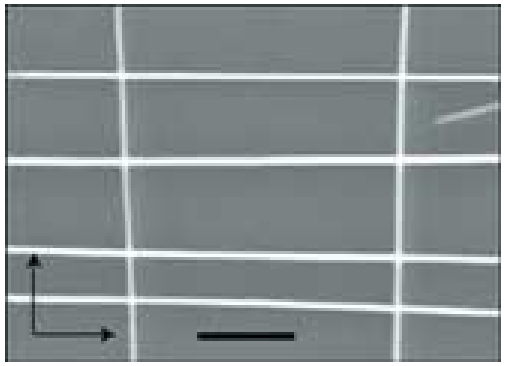
Metrology & Molecular Electronics





James Heath, Fraser Stoddart, and Anthony Pease

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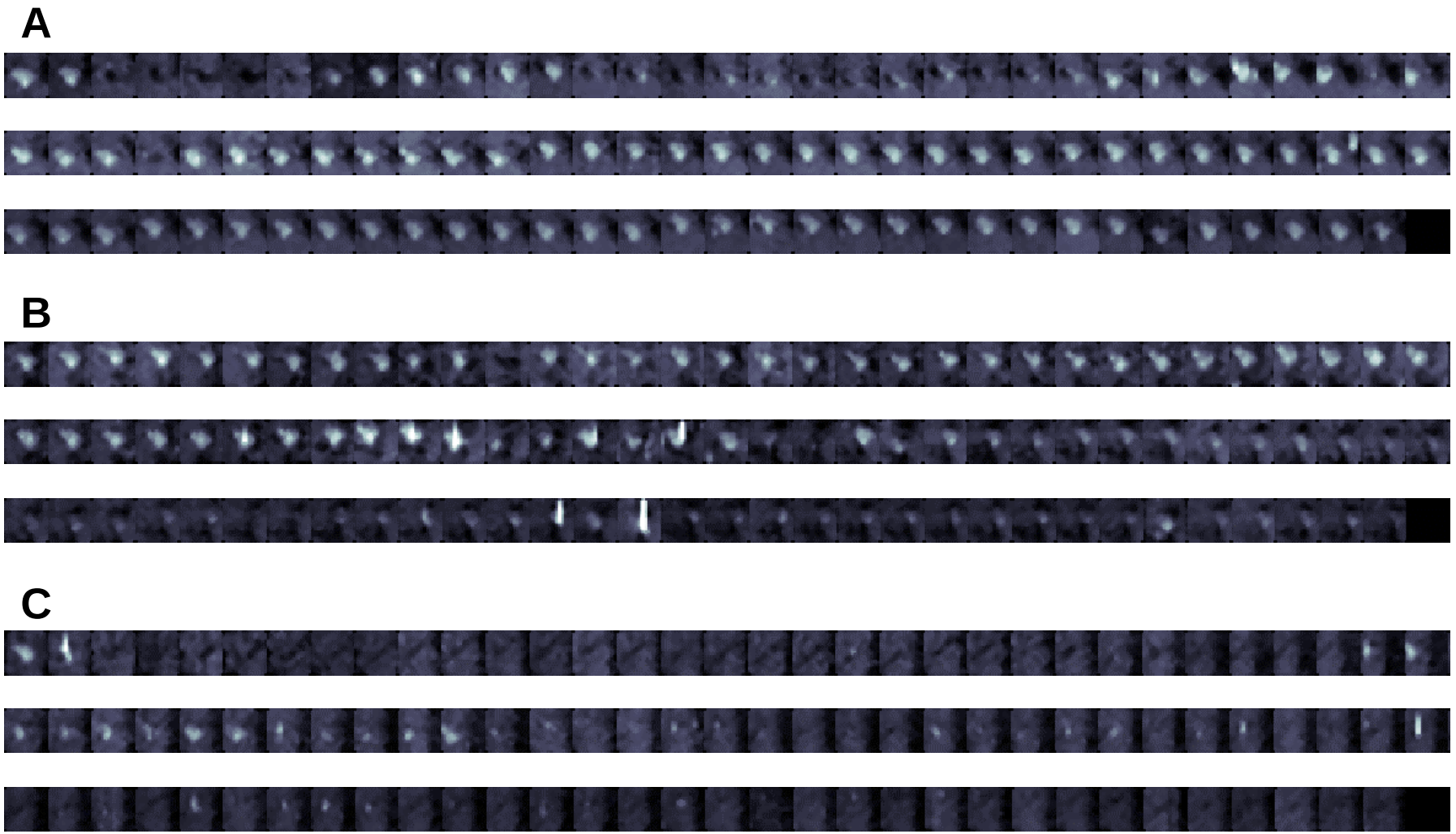
Metrology & Molecular Electronics



Paul Weiss's Group – STM of Conductance Switching

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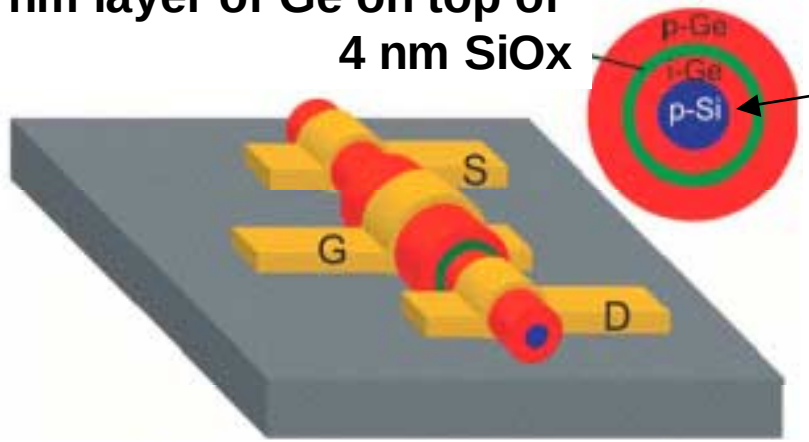
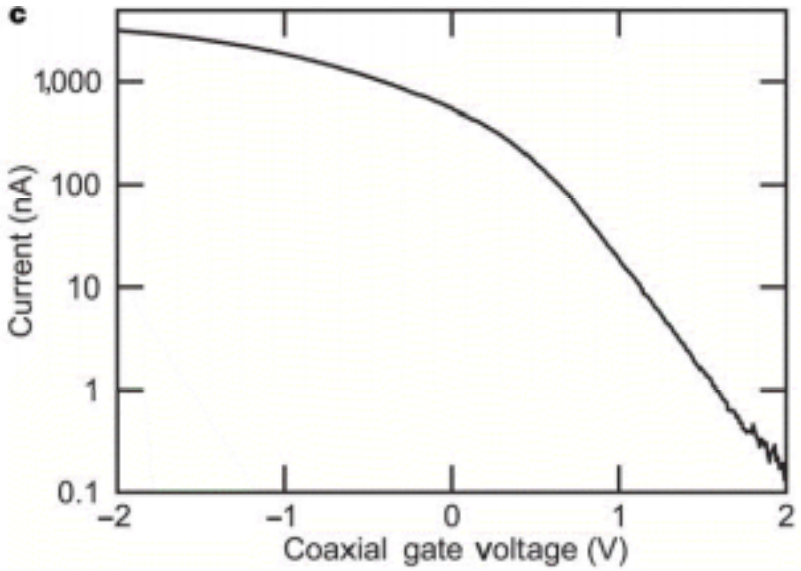
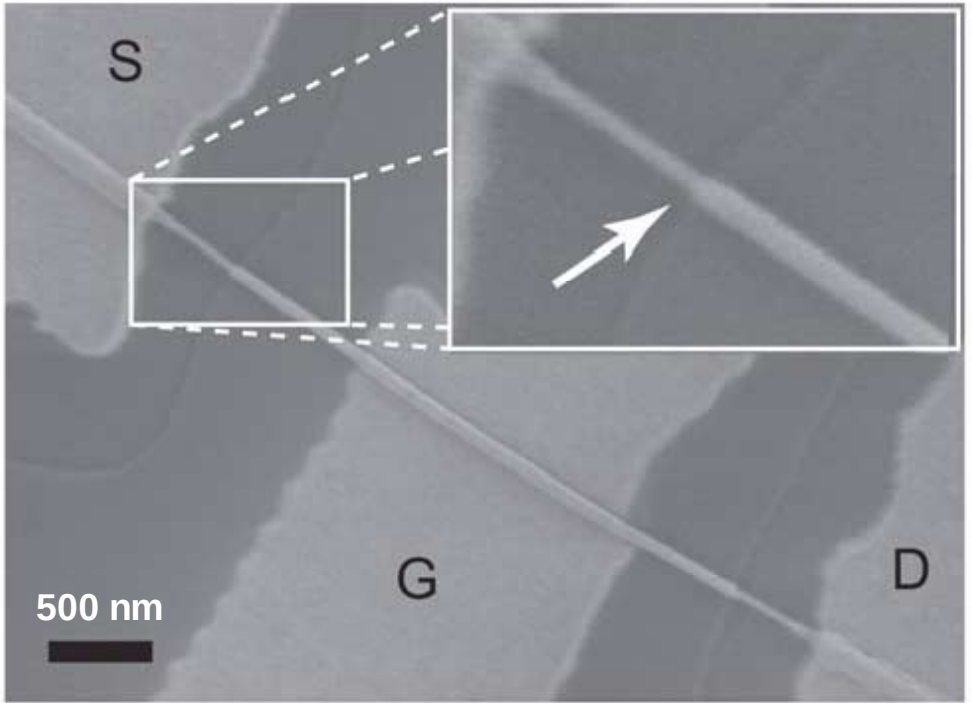
Nanowire Transistors and Interconnect

5 nm layer of Ge on top of 4 nm SiOx

10 nm p-Si core diameter & 10 nm i- Ge layer







L.J. LAUHON, M.S. GUDIKSEN, D. WANG & CHARLES M. LIEBER
***Nature* 420, 57 - 61 (2002)**

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Conclusions

- **There are many opportunities for the Physics Community in the area of future IC technology**
- **Nanoelectronics is here!**
- **Metrology is a Key Enabler!**

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Use of HRTEM for Calibration

High Resolution TEM (Phase Contrast) has a ~ 10% error for Thickness Determination Due to Cs

Specimen Thickness A	Specimen Tilt (mrad)	Defocus	Cs (mm)	Oxide Model Thickness	Oxide Measured Thickness	% Error
154	0	-425	0.5	10.56	9.84	-6.8
154	0	-156	0.5	10.56	11.4	8
154	0	-20	0.5	10.56	10.44	-1.1
154	12.6	-425	0.5	10.56	9.12	-13.6
154	25	-425	0.5	10.56	10.68	1.1
154	0	-425	0.5	10.56	8.88	-15.9

HRTEM Image Simulations for Gate Oxide Metrology

S. Taylor, J. Mardinly, M.A. O'Keefe, and R. Gronsky

Characterization and Metrology for ULSI Technology 2000

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